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DESIGN AND DEVELOPMENT OF A TELEMETRY LOGGING SYSTEM.(U)
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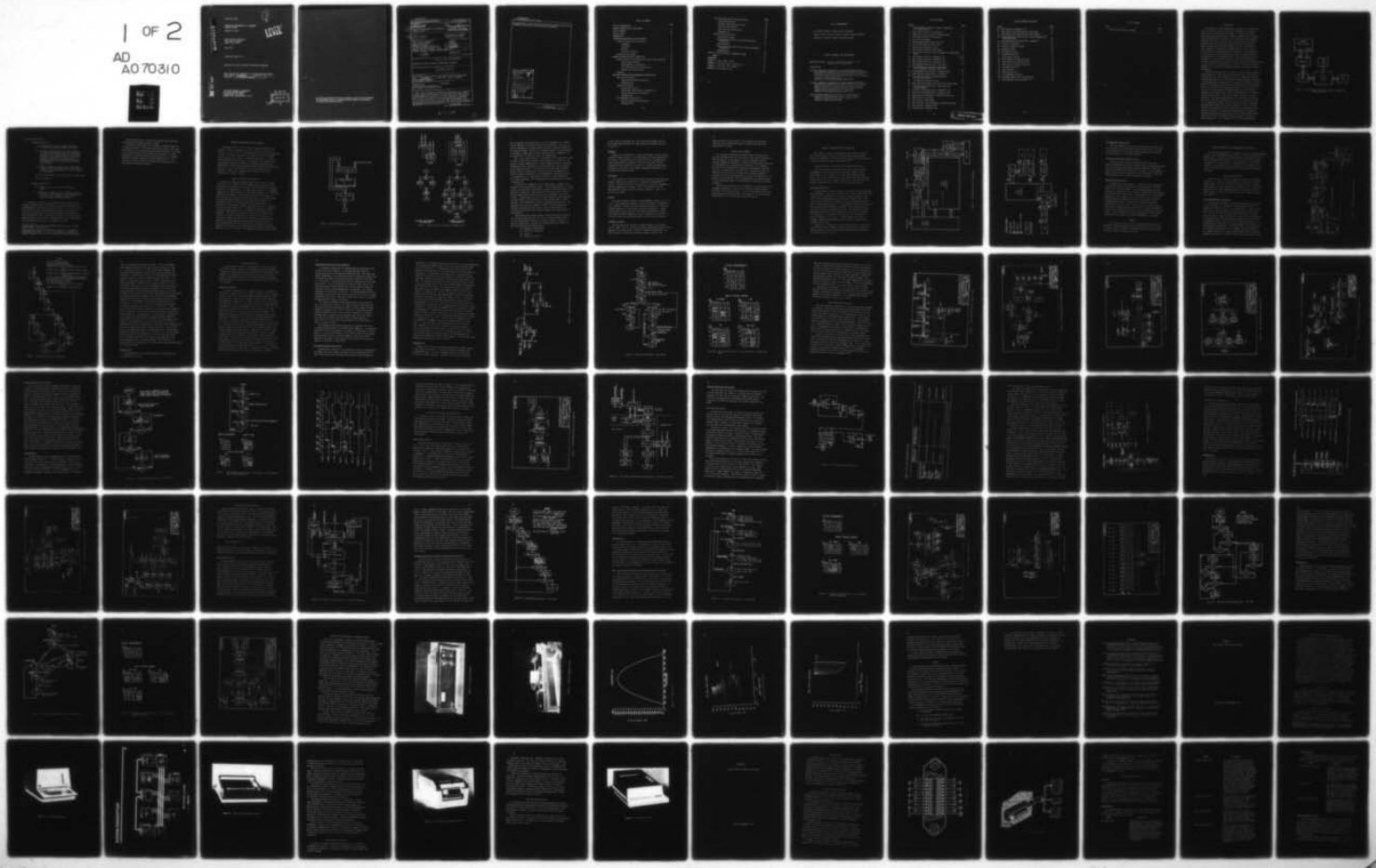

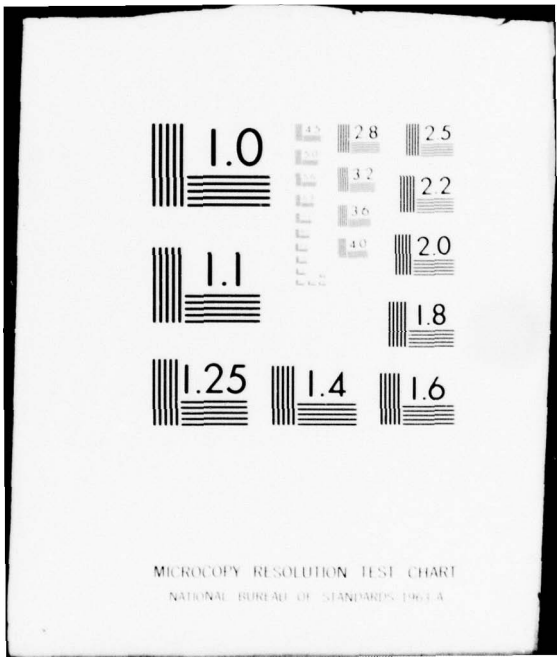
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AFGL-TR-78-0180

DESIGN AND DEVELOPMENT OF A TELEMETRY LOGGING SYSTEM

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Scientific Report No. 2

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report documents the design and development of a telemetry logging system that formats and records analog and digital data from rocketborne instruments. The main objective in the development of this system was to improve data acquisition capability so on-the-spot data plots of the instrument measurements would be available for quick-look analyses. The system design includes

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an explanation of the controller-subcontroller design concept with schematic illustrations and processed data samples.

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LIST OF CONTRIBUTORS

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David A. Burt, Assistant Director, Space Science Laboratory

William I. Fletcher, Digital Systems Laboratory

RELATED CONTRACTS AND PUBLICATIONS

DNA 001-76-C-0256: *In situ Measurements in Support of the Wideband Satellite Experiment*

Publications:

Air Force Geophysics Laboratories, Stanford Research Institute and Utah State University, *Quick Look Field Report Coordinated Investigation at High Latitude Scintillations by Wideband Satellite, Chatanika Radar and Sgt-Hydac Multi Rocket Conducted 08:10:50 UT on 28 February 1978,* submitted to DNA Program Manager, March 1978.

Air Force Geophysics Laboratories, Stanford Research Institute and Utah State University, *Quick Look Field Report Coordinated Daytime Investigation of High Latitude Scintillations by Wideband Satellite, Chatanika Radar and Honest John-Hydac Wideband Rocket Conducted 1906 UT 1 March 1978,* submitted to DNA Program Manager, March 1978.

Space Science Laboratories, USU, *Quick Look Field Report Equatorial Irregularities-Wide Band Satellite Support Conducted Kwajalein Missile Range 23 August 1977,* submitted to DNA Program Manager.

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INTRODUCTION

A need exists in rocket measurements programs for a system that can be used in the field for quick-look evaluation of the results from the various rocketborne instruments. In the past the data evaluation has usually involved a limited preliminary effort of manually reading analog strip charts in the field with a more complete evaluation after the field party had returned to home stations and telemetry tapes were processed through the routine data systems. These systems suffered from the handicap that the in-field strip chart examination could not be thorough enough to provide the sufficient input to program managers and scientists. The completion of the second phase necessarily involves a delay of several months in getting material into presentable form. This report details the development of a field-portable system for interfacing the output of a rocket telemetry data acquisition system to microprocessor-based graphics system for processing and plotting the results soon after the rocket flights so they can be quickly made available to interested scientists and managers.

The quick-look data system is based on a Tektronix^{R} 4051 Graphics System along with a 4662 Interactive Digital Plotter, a 4924 Digital Cartridge Tape Drive and a 4631 Hard Copy Unit. Appendix A contains a general description of the 4051 Graphics System and these peripherals. A block diagram of the system with its peripherals is shown in Figure 1. The 4051 has enough calculating power to process and plot the results, either on its Direct View Storage Tube (DVST) or on the 4662 Plotter, of most of the experimental instruments made by the Space Science Laboratory providing the data from these instruments can be stored and then fed into the 4051. Since a mass storage capability is often required for this data logging function, the 4924 Digital Cartridge Tape Drive, which can be operated in an "on line" mode with the 4051 or in a "stand alone" mode, is ideally suited to these requirements. The remaining obstacle and the major thrust of the effort reported here was the development of the interface from the telemetry ground station to the 4924. Generally, the interface must be capable of transferring either analog or digital data from the telemetry ground station to the 4924 in a standard format along with the data for time determination. The following are the detailed requirements

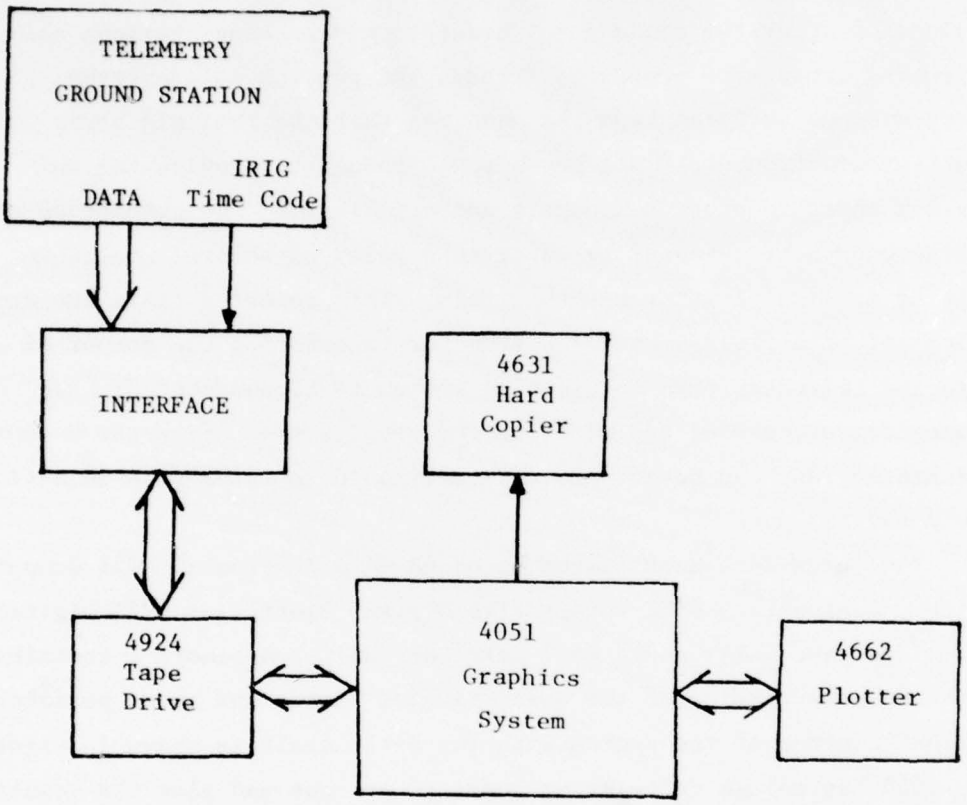

Figure 1. Block Diagram of Complete Telemetry Logging and Processing System

of the interface system:

Primary Requirements

(1) Compatible with the 4051 Graphics System via the GPIB[1] 4924 Digital Cartridge Tape Drive.

(2) Capable of logging from one to eight channels* of analog data from the telemetry ground station (at input levels ranging from 1 volt to 15 volts adjusted to an acceptable range for the analog-to-digital convertor) at a constant rate*, formatted with data for time determination from the standard IRIG[2] time codes available at the launch ranges.

(3) Capable of logging a single serial digital data channel from the telemetry ground station with the interface self-synchronizing to the sync word* and the data frame*.

(4) Field operational with a 117 volt, 60 Hz power source.

(5) Rack mountable.

Secondary Requirements

(1) Simple for the user to both understand and operate.

(2) High input impedance to the interface with input protection in the interface. (The input protection is both for device protection and cross-talk protection due to the CMOS circuitry.)

In order for the 4051 to have meaningful data to work with, the interface transfers data to the 4924 at a constant rate with time determining data that includes the IRIG time code at the first of the tape and special mark bytes throughout the tape. By so doing, the time of a particular data byte can be determined and coordinated to the trajectory plot (also calculated by the 4051) to find corresponding altitude for the data byte. Programs written on the 4051 process the data and plot the results on the DVST or the 4662.

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[1] General Purpose Interface Bus--Standard bus structure for the 4051, 4662 and 4924. See Appendix B.

[2] Inter-Range Instrumentation Group--Group that defines standard for instrumentation signals. For time code standard, see Appendix C.

*Implies parameters that must be user-selectable from the front panel.

Using this process, a versatile and valuable quick-look data acquisition and processing system is formed.

The thrust of this report is to present the design concept of the interface system. The system is relatively unique in the sense that instead of the traditional single system controller, it contains a main system controller with several subcontrollers to perform operations for the main controller much the same way as a software subroutine performs a task for the main program routine. This technique, called the controller-subcontroller design concept, is discussed and illustrated in detail.

CONTROLLER-SUBCONTROLLER DESIGN CONCEPT

The design concept for this system is unique although not new. William I. Fletcher introduces the idea in his text *An Engineering Approach to Digital Design* to be published by Prentice-Hall Incorporated in 1979. This report illustrates and supports, as well as defines certain aspects of the concept. Emphasis in this report is placed on the system level of the design. The design of the controller and subcontrollers generally follows the procedures and architectures established for finite state machines and multi-input system controllers in Chapters 6 and 7 of Fletcher's text. They are therefore not presented in this report although a block diagram of the basic architecture is shown in Figure 2.

Controller-Subcontroller Approach

Inherent to almost any digital system is the need for a system controller. This controller causes another device, external to the controller but contained in the system, to perform one of its inherent functions to accomplish part of a system level operation. For example, assume that the device external to the system controller is a 74194 4-bit universal shift register. The controller can cause this device to perform a parallel load, shift right, shift left, or do nothing simply by controlling three inputs (clock, S1, S0) into the device. As previously stated, the system controller is using the device to perform one of the device's inherent functions in order to accomplish one of the system's operations. To emphasize this concept, suppose a controller contained two set-reset flip-flops that are not interconnected. The system is required to perform a two-bit shift right or shift left operation with these two flip-flops. In Figure 3 a comparison is shown between this case and the previously mentioned case where a system controller uses an external shift register. It can be readily seen that the operation of the controller is greatly complicated by requiring it to perform the shift register's operation; and this is only for two bits! This example is based on a rather simple

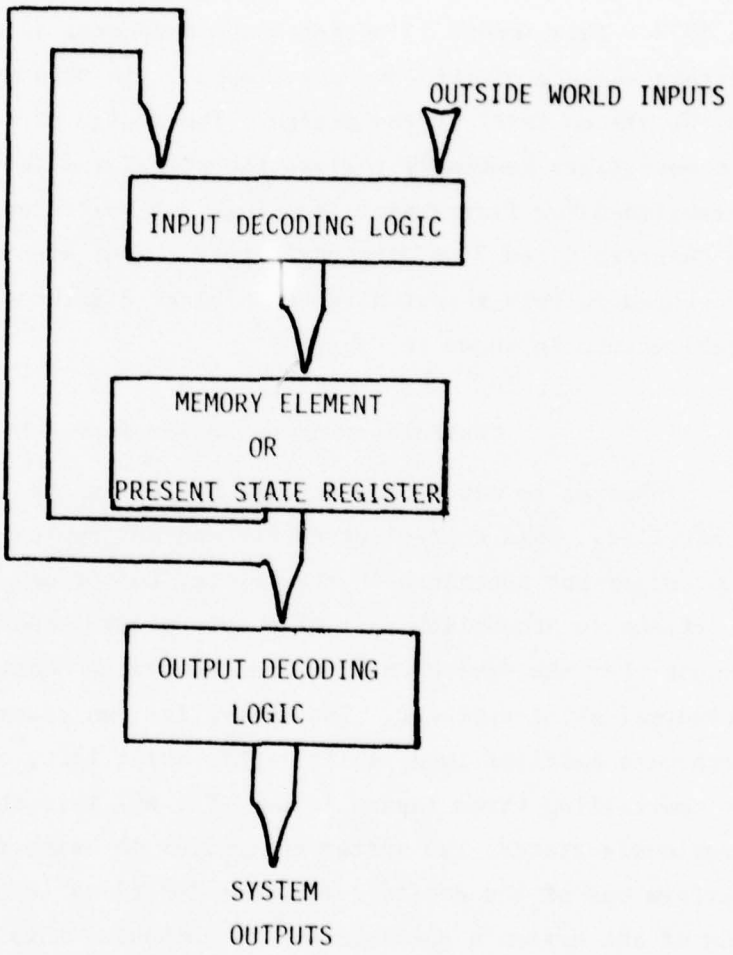
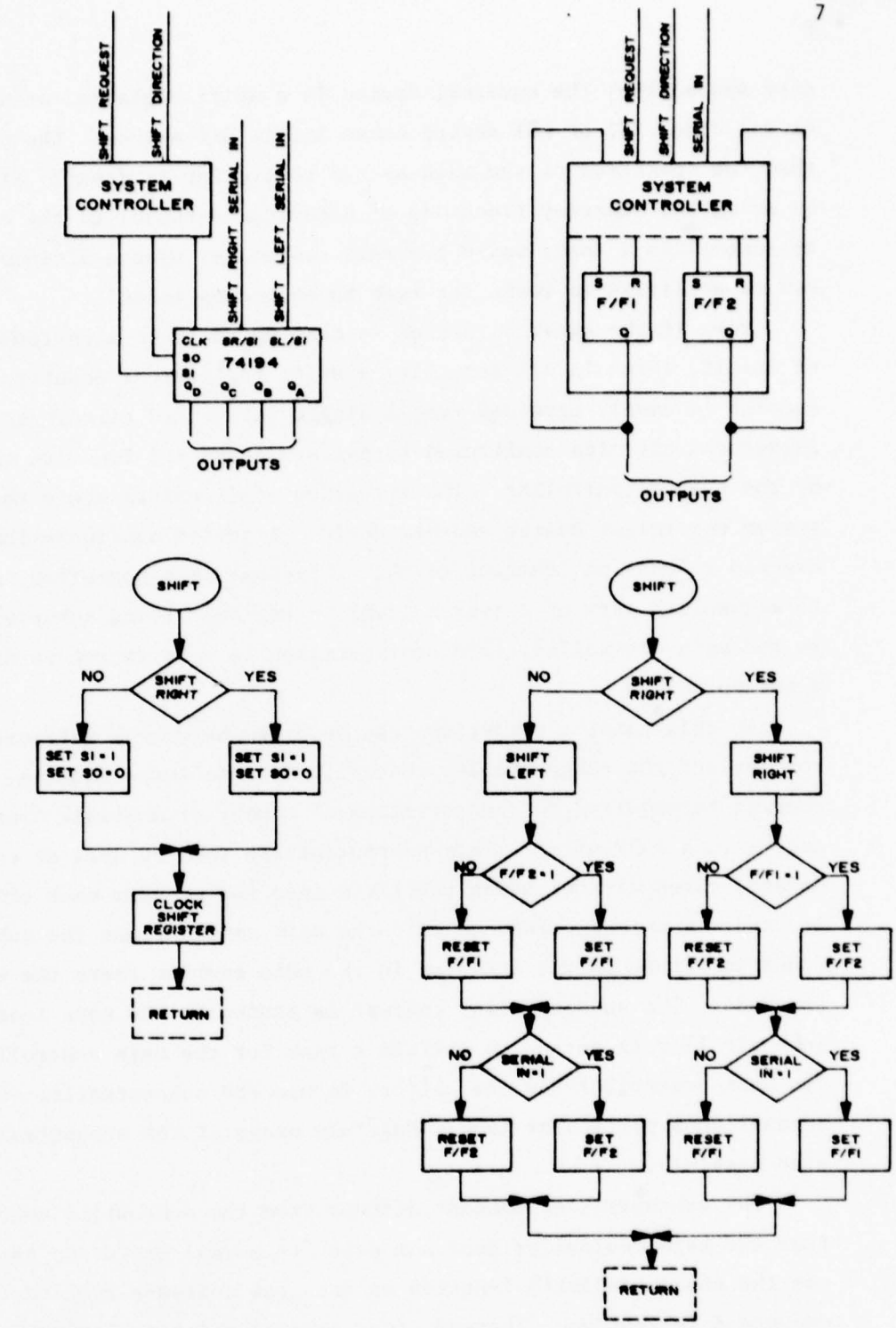


Figure 2. Basic Architecture of a Controller



EXTERNAL SHIFT REGISTER IMPLEMENTATION

INTERNAL FLIP-FLOP IMPLEMENTATION

Figure 3. Comparison of Shift Register Implementations

case and whether the external device is a shift register, or a counter or any other MSI or LSI device makes little difference. The point is that the operation of the main system controller is greatly simplified by using the inherent functions of a device, external to the controller, to accomplish a task, while the main controller uses a minimum of its own capabilities to cause the task to be accomplished.

Now, if the external device is considered to be a controller in and of itself, which in all actuality a shift register or counter is, the concept is easily expanded from a single integrated circuit to multiple integrated circuits configured to perform a special function required by the system controller. The situation still exists where the main system controller causes another device or device configuration to execute a function inherent to the configuration's operation in order to accomplish part of a system level operation. Being subservient to the main controller, this configuration is more appropriately called a subcontroller.

At this point a comparison can be drawn between a software subroutine and the subcontroller concept. In a software routine, if a short routine is required for conservation of memory or multiple usage, it is made into a subroutine. This subroutine can then be used or called several times without being rewritten into the program each time it is used. A method exists to exit the main routine, use the subroutine, and then return to the location in the main routine where the exit was made. The subcontroller concept is basically the same idea. The subcontroller is set up to perform a task for the main controller. The main controller has the ability to use the subcontroller to accomplish a particular task. Multiple usage of the subcontroller is also possible.

The subcontroller concept differs from the subroutine concept in that the main controller does not exit its normal execution path to use the subcontroller's function as does the software routine to execute a subroutine. Instead, four schemes exist to interface the main controller and the subcontroller:

(1) Handshake (closed loop)

(2) Initiation (open loop)

(3) Monitor

(4) Transfer of control

To this author's knowledge these four interfacing schemes have not been established previously by other authors and therefore will now be defined.

Handshake

Basically the handshake is a closed loop scheme in which the main controller issues a signal to the subcontroller to begin execution of its routine. The main controller then waits for the subcontroller to return a signal as an indication to the main controller that the subcontroller has completed its operation. The main controller then continues its operation. More complex handshake schemes exist, but are based on the same principle.

Initiation

The initiation is an open loop scheme in which the main controller issues a signal to the subcontroller to begin the subcontroller's routine. The main controller then continues its operation transparent to what the subcontroller is doing. There is no provision for the subcontroller to send a pulse to the main controller. Thus, it is an open loop scheme.

Monitor

The monitor scheme is similar to the handshake scheme in that it is a closed loop scheme and the main controller initiates the subcontroller's operation. However, the main controller continues its operation without waiting for a return signal from the subcontroller. Should a return signal occur, the controller takes the appropriate action. This scheme is usually employed to "watch" or monitor the operation of a circuit, such as data synchronization, and thus derives its name.

Transfer of Control

The function of the transfer of control scheme is self-evident from its name. That is, the main controller relinquishes control of the system to the subcontroller. Control is usually not returned to the main controller. This type of scheme is used at a place in the

main controller's routine where it has completed all functions required of the system other than the functions involved in the subcontroller's routine.

Design Concept Summary

The controller-subcontroller design concept is based on the idea that subcontrollers can be used with a main system controller in much the same way as subroutines are used in software routines. Different schemes are available to interface the main system controller to the subcontroller, giving greater flexibility to the designer. The speed of the system may be increased by allowing more than one function to be performed at the same time. The design concept also simplifies the system both in design and in hardware complexity. A system can be built in subcontroller sections, and additions to the system can be facilitated. These advantages are increased even more if there is multiple usage of a subcontroller's function by the main controller.

Using this design concept it is important to clearly establish the handshake scheme that is to be used to interface the main system controller to the subcontrollers. If this is done during the initial design phase and followed through, interfacing of the controller and subcontroller(s) can be done with minimal difficulty.

GENERAL SYSTEM FUNCTIONAL DESCRIPTION

This chapter provides a general functional overview of the system. The function of the main system controller and each subcontroller are introduced. This chapter also illustrates the interaction of the main system controller and subcontrollers.

System Controller and Subcontrollers-Functional Overview

Using the previously described design concept and the system requirements, the functional partition, shown in Figure 4, was established for the interface to the 4924 Digital Cartridge Tape Drive. The system is comprised of a main system controller and three subcontrollers: the GPIB handshake subcontroller, the IRIG time code decoder and subcontroller, and the digital data subcontroller.

Main System Controller

The main system controller interprets settings from the front panel and accordingly, controls the operation of the system. When a function of one of the subcontrollers is required, the main controller uses one of the four handshake schemes described in Chapter Two to avail itself of the subcontroller's function. This is illustrated in the Control Flow Diagram in Figure 5. The analog data routine is integrated into the main system controller since part of the analog routine is also part of the main controller's routine. The analog data routine multiplexes from one to eight channels (as set on the front panel) of analog data at a constant rate (also set on the front panel for rates of 2^n where n = 1 to 11 or 1 to 2048 samples per second) through a sample and hold amplifier and an analog-to-digital (A/D) convertor to the GPIB.

Analog data is formatted with three binary bytes of the time code at the first of the file (hours, minutes, and seconds), a mark byte (240 in binary), and then the digitized analog data with a mark byte after every 210 bytes of data.

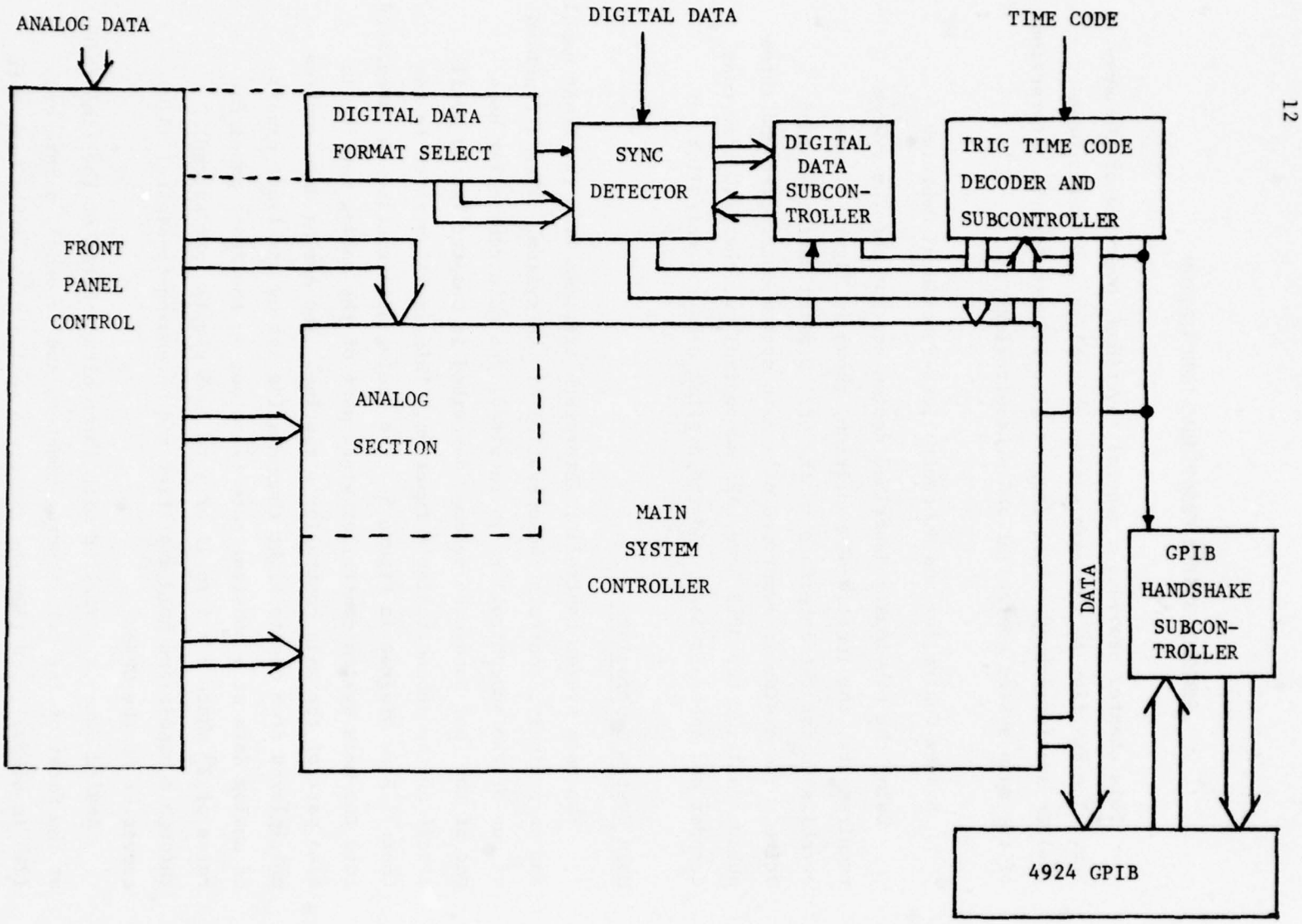


Figure 4 Functional Partition of Interface

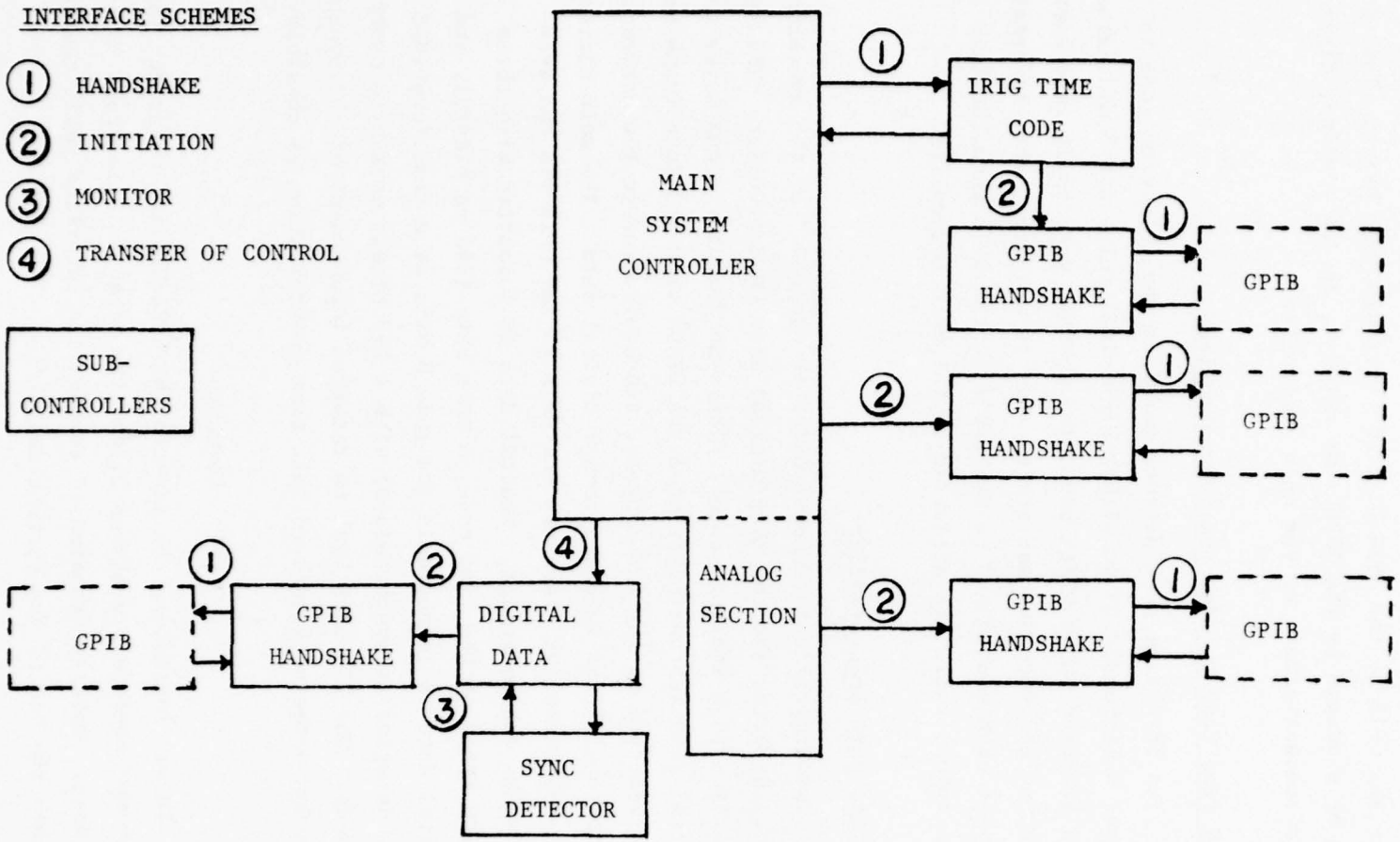


Figure 5. Control Flow Diagram

GPIB Handshake Subcontroller

The GPIB handshake subcontroller transfers data in 8-bit bytes over the GPIB to the 4924 Digital Cartridge Tape Drive. This data can be produced by the IRIG time decoder, analog routine, digital data subcontroller, or the main controller.

IRIG Time Code Decoder and Subcontroller

The IRIG time code decoder receives the IRIG time code in format B (Appendix B) in either sinusoidal pulse width modulated (PWM) or a detected pulse width modulated format, decodes it into hours, minutes, and seconds, and stores this in a latch. This information is updated each second and is available to the GPIB when the IRIG time code subcontroller is activated by the main controller.

Digital Data Subcontroller

The digital data subcontroller is comprised of the synchronized (sync) detector and the main digital data subcontroller. The two interface in a monitor scheme. The sync detector signals the main digital data subcontroller when the SYNC[1] word and data frame boundries, both selected on the front panel, are equivalent to the corresponding parameters of the incoming serial digital data. The main digital data subcontroller transfers the data to the GPIB via the GPIB handshake subcontroller. Digital data is formatted with three binary bytes of the time code, a mark byte (240 in binary), and then digital data is logged onto the tape 8 bits at a time (provided the sync detector is synchronized) with a 253 binary mark byte every four seconds. The 253 mark byte is recorded independent of the synchronization detector signal so that time determination is possible.

Comments

In all instances, the tape in the 4924 Digital Cartridge Tape Drivemust contain pre-marked files with adequate file space to store the data. Data is transferred through the interface until the tape reaches the end of the current data file.

DETAILED CONTROLLER AND SUBCONTROLLER DESCRIPTIONS

The main system controller is designed to incorporate the analog data routine. The GPIB handshake subcontroller, IRIG time code decoder and subcontroller, and digital data subcontroller are designed to interface to the main system controller by using one of the four schemes introduced in the Design Concept. The details of the main system controller, each subcontroller, and interfacing are explained in this chapter. The detailed functional partition of the system is shown in Figure 6.

Main System Controller

The main system controller interprets the front panel settings relative to its operation and accordingly, activates the necessary subcontrollers. The two front panel settings that affect the main system controller are the pushbutton time code switch with which the user initiates the data logging operation of the system, and the rotary switch to select the digital data channel or number of analog data channels.

Detailed Operational Description

The flow chart in Figure 7 describes the operation of the main system controller. The controller is initialized to state "a" with either a power-up reset or an external reset. It waits in this state for the time code switch to be pushed and then enters state "b". In state "b" the controller causes three bytes of the IRIG time code (hours, minutes, and seconds) used for time determination, to be transferred to the 4924 Digital Cartridge Tape Drive by using a handshake interface scheme to the IRIG time code subcontroller. The subcontroller then uses an initiation scheme to interface to the GPIB handshake subcontroller. The digital time code is selected on the output multiplexer and the data transfer is initialized with H.S. ENABLE being set and a pulse from the sample clock to the GPIB handshake subcontroller. When the three bytes are recorded, the IRIG

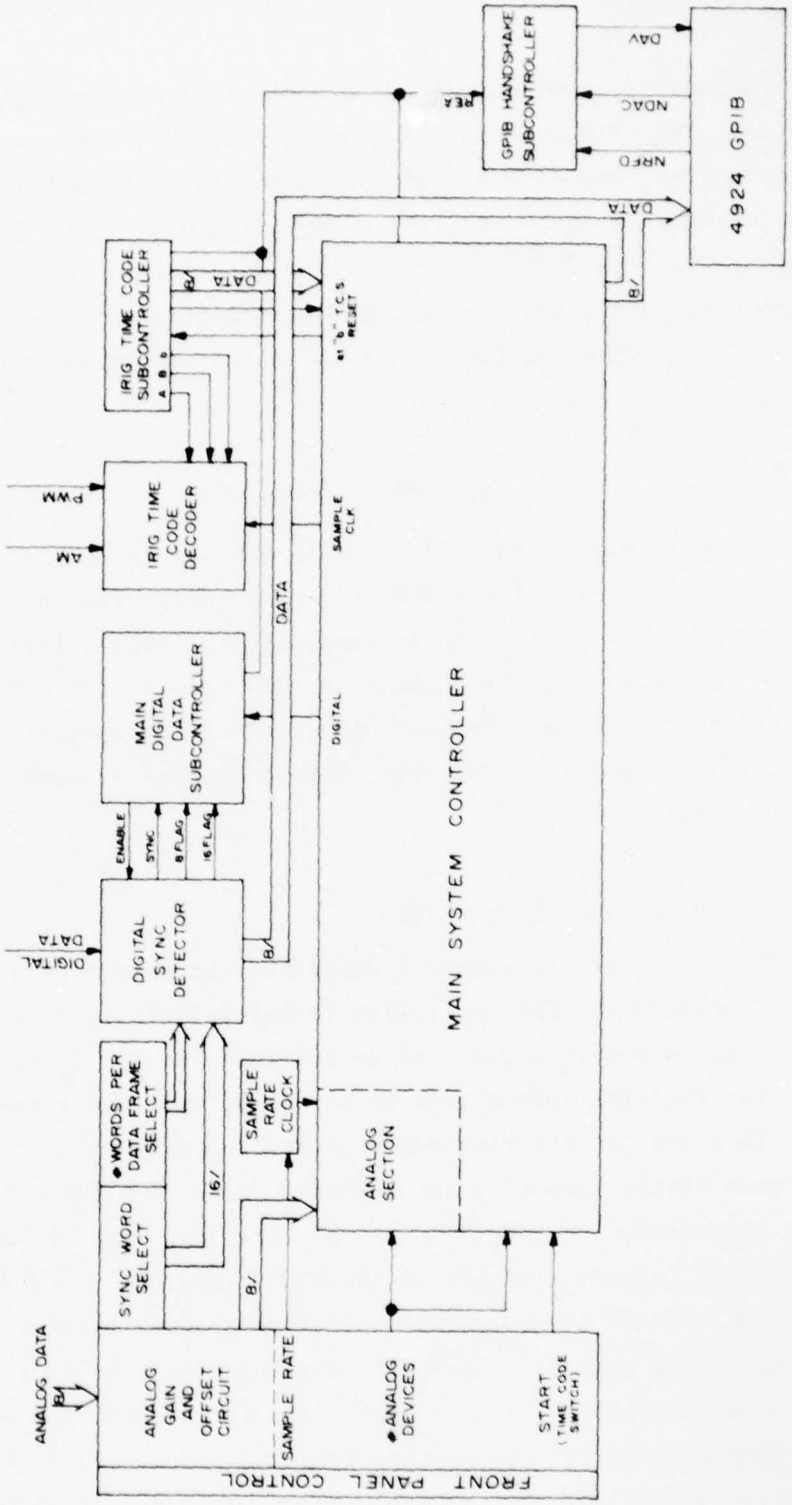


Figure 6. System Detailed Functional Partition

LEGEND

T.C.S.: Time Code Switch
H.S. EN.: Handshake Enable
STATUS MUX: Status Multiplexer
OUT MUX TO TM.: Output Multiplexer selects time code.
OUT MUX TO MK.: Output Multiplexer selects mark byte.
OUTMUX TO ALG: Output Multiplexer selects digitized analog data.
st "A": state A of GPIB Handshake subcontroller.
st "D": state D of GPIB Handshake subcontroller.
BYTE CNTR: Data Byte counter.
C.M. CNTR: Commutator counter.
C.M. Setting: Commutator equals front panel setting.
ANALOG: Front panel analog channel switch.

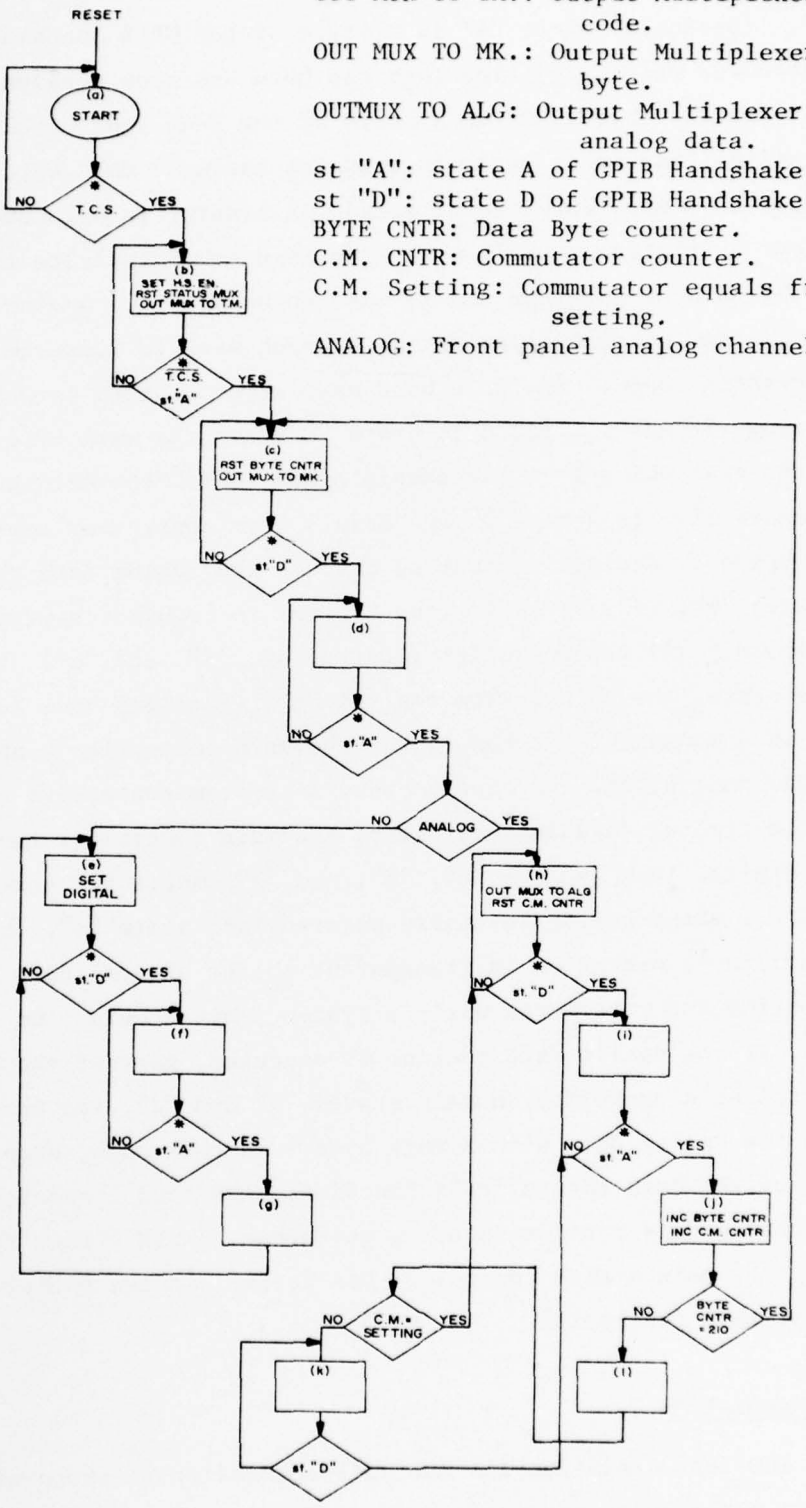


Figure 7. Main System Controller: Flow Chart

time code subcontroller resets T.C. SWITCH. With this handshake return signal and state "A" the main controller advances to state "c". (Basically state "A" is a state of the GPIB handshake subcontroller which signifies that the data has been received by the GPIB device. State "D" is a state of the same subcontroller which signifies that it is ready to transfer the next data byte.) In state "c" a mark byte, equal to 240 in binary, is selected on the output multiplexer. This mark byte is used to indicate the start of the data on the tape and is used throughout the analog routine to aid in time determination and as a bench mark to increase the data processing speed. The GPIB handshake subcontroller is still functioning (it was initiated in state "b") and the mark byte is transferred on the next pulse from the sample clock. With the GPIB handshake subcontroller in state "D" the main system controller moves to state "d" where it decides whether to execute the analog data routine (states "h", "i", "j", "l", and "k") or to transfer system control to the digital subcontroller (states "e", "f", and "g"). After this state, the main system controller's functions have been completed and in a sense this is the end of the main controller's operation as a main controller. In other words, if system control is transferred to the digital data subcontroller, the main controller remains in the digital loop (states "e", "f", and "g") until the system is reset. However, after having initially entered into state "e", the main controller's operation is transparent to the digital data subcontroller's operation and vice versa until a system reset occurs. On the other hand, if the analog data routine is executed, part of the main system controller's operation, namely states "a" and "d", are used in formatting the analog data with a mark byte. In this case, even though part of the main controller's functions have been completed, only the analog data routine is being performed. With either type of data, the main system controller has no part in the operation functioning as the main controller.

Implementation

The implementation for the main controller is shown with that of the Analog Data routine.

Analog Data Routine

The analog data routine is incorporated into the main system controller's routine. That is, the formatting part of the routine is done in the main controller's routine while the analog data logging capability is contained in an extension of the main controller's routine. Some analog circuitry is required to adjust the incoming analog signal(s) to a range that can be handled by the other circuitry of the system.

Operational Overview

In order to record data at a constant rate, as is required for the system, a sample rate clock is used to indirectly pace the analog routine. This clock controls the sample and hold integrated circuit and the analog-to-digital (A/D) convertor which in turn causes the GPIB handshake subcontroller to transfer the data to the 4924 Digital Cartridge Drive. (This is shown later with the GPIB timing diagram in Figure 16.) The available sample clock rates are 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 128 Hz, 256 Hz, 512 Hz, 1024 Hz, and 2048 Hz (should only be used for short files $\leq$ 512 samples). The analog data routine itself is basically a formatting routine whose operation is dependent on the operation of the GPIB handshake subcontroller. In this way the sample rate clock indirectly paces this routine. After each digitized analog data byte has been recorded, the analog data routine selects the next analog channel (via the commutator counter (C.M. counter)) that is to be sampled and digitized. It also increments the byte counter. When the C.M. counter is equal to the setting on the front panel switch used to select the number of analog devices, the counter is reset and the sampling sequence starts again. After 210 data bytes are recorded, the mark byte (240) is recorded, the byte counter and the C.M. counter are reset, the routine returns to recording digitized analog data. Two hundred ten was chosen because an entire sequence of 1, 2, 3, 5, 6, or 7 channels can be recorded before a mark byte is recorded. This process continues until the end of the current tape file on the 4924 is reached.

Analog Data Input Control and Regulation

An important prerequisite to transferring the analog data is the setting of the input signal(s) to standard amplitude limits for scaling and control of the digitized numerical value. The lowest and highest amplitudes of the analog signal must be adjusted to levels that are within the range of the analog-to-digital convertor (0.00 volts to + 10.0 volts). The digitized data must be compatible with the 4924 and the 4051. It is also desirable to keep the binary value of the digitized data well below the mark byte (250 in binary) so that the integrity of this time determining data is preserved. The voltage equivalent of binary 240 is 9.38 volts. It was determined that little resolution is lost if the upper binary limit is set at 210 or a voltage equivalent of 8.20 volts. The lower binary limit is set at 0 with its voltage equivalent equal to 0.00 volts.

Data from the telemetry ground station enters the interface as an a.c. signal with no offset. The upper and lower limits vary with the site location and discriminator levels. Typical ranges for these signals are anywhere from ±1 volt to ±10 volts. The data from some telemetry ground stations is also inverted. Therefore, the analog gain and offset controls of the system must have sufficient range to allow the user to adjust the input signal of these ranges to a lower limit of 0.00 volts and an upper limit of 8.20 volts with an option to invert the data.

The incoming analog signal(s) must also be regulated so as not to exceed the power supply of the CMOS analog commutator. The signal(s) should also be current regulated to decrease the cross-talk in the commutator. A circuit that fulfills all of these criteria for the analog gain and offset circuit is shown in Figure 8. The circuit can be adjusted to the proper output value of 0.00 volts to 8.2 volts for an input of ±0.50 volts to ±15.00 volts.

Detailed Operational Description

Explaining the operation of the analog data routine in more detail, the sample rate clock strobes the sample and hold integrated circuit with a short pulse from a monostable multi-vibrator and initiates the

conversion of the analog-to-digital (A/D) convertor with the STROBE pulse. The rising edge of STROBE resets the convertor and the falling edge starts the conversion. The STATUS line of the A/D convertor goes high with the rising edge of the STROBE pulse and returns low when the conversion is finished about 30 μseconds later. This high-to-low transition is used in an initiation scheme to interface to the GPIB handshake controller which transfers the digitized analog data to the 4924. The analog routine monitors states "A" and "D" when the 4924 is not accepting any data. Each time the GPIB handshake subcontroller goes from state "D" to state "A" a data byte has been recorded and the analog routine increments the commutator counter and the byte counter. As shown in the flow chart in Figure 8, state "h" of the analog routine causes the output multiplexer to select the digitized analog data and resets the commutator counter to zero. It waits in this state for the GPIB handshake subcontroller to enter state "D" and then moves to state "i". In state "i" the routine waits for the subcontroller to enter state "A", signifying that the 4924 has received a data byte. In state "j" the commutator counter and the byte counter are incremented. If 210 data bytes have been recorded, the routine returns to state "c" where a mark byte is recorded and then the analog routine is re-entered. If less than 210 data bytes have been recorded the routine goes to state "l". In this state the commutator count is compared to the number of analog data channels set on the front panel. If they are equal, the routine returns to state "h" where the commutator count is reset to zero and the routine continues. If they are not equal, the routine goes to state "k", waits for state "D", and then returns to state "i" to continue the routine. The key to the analog routine is the monitoring of the GPIB handshake sub-controller and making the changes in the commutator selection and output multiplexer only between states "A" and "D".

Implementation

Figures 9 and 10 show the Mnemonic Designated State (MDS) diagram of the flow chart in Figure 7, along with the state assignment map and NEXT STATE maps. The state assignment is made for D flip-flops as the state holding register. Since state "A", state "D", and the

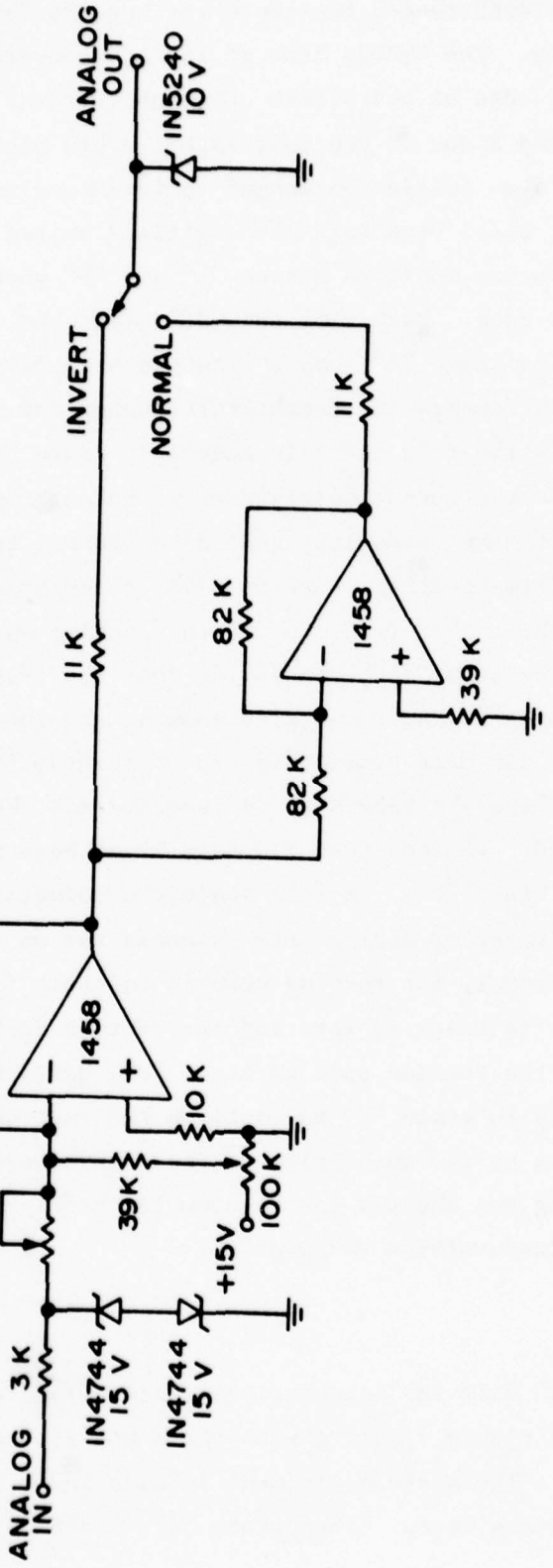


Figure 8. Analog Gain and Offset Circuit

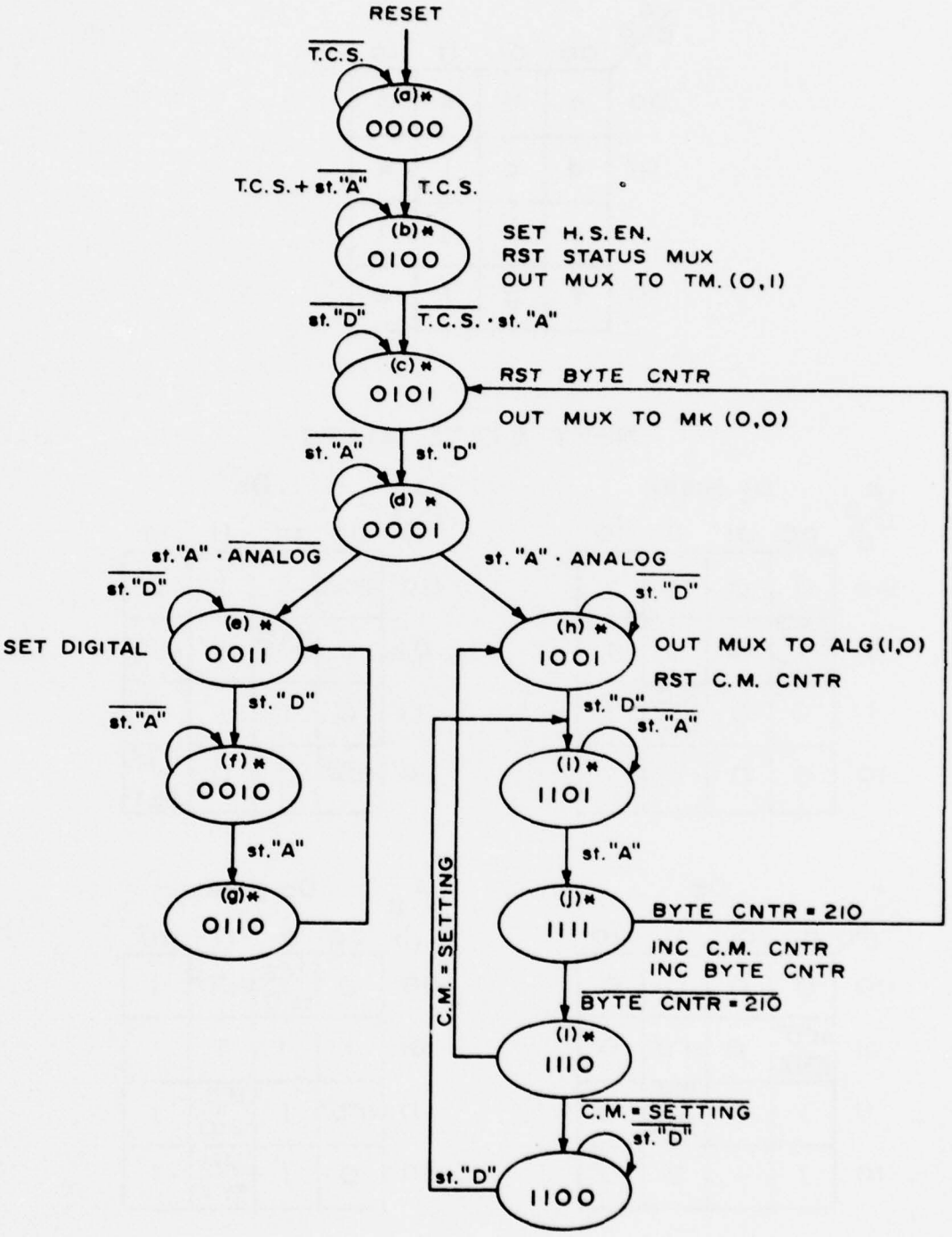


Figure 9. Main System Controller: MDS Diagram

STATE ASSIGNMENT

CD \ AB	00	01	11	10
00	a	b	k	Ø
01	d	c	i	h
11	e	Ø	j	l
10	f	g	l	Ø

NEXT STATE MAPS

D_A (MSB)

CD \ AB	00	01	11	10
00	0	0	1	1
01	st."D" · ANA	0	1	1
11	0	0	$\overline{B.C.=210}$	1
10	0	0	1	1

D_B

CD \ AB	00	01	11	10
00	T.C.S.	1	1	0
01	0	$\overline{st."D"}$	1	st."D"
11	0	1	1	0
10	st."A"	0	0	$\overline{C.M.=SET}$

D_C

CD \ AB	00	01	11	10
00	0	0	0	0
01	st."D" · $\overline{ANA}$	0	st."D"	0
11	1	0	$\overline{B.C.=210}$	0
10	1	1	0	0

D_D (LSB)

CD \ AB	00	01	11	10
00	0	T.C.S. st."D"	st."D"	1
01	1	1	1	1
11	st."D"	1	B.C. = 210	1
10	0	1	C.M = SET	1

Figure 10. Main System Controller: State Assignment and NEXT STATE Maps

time code switch are essentially asynchronous variables to this controller, all NEXT STATE assignments are unit distance from present states that branch off of these variables. Also, with the exception of state "d", present states that branch off of these variables are only concerned with one variable for their branching. In state "d" two variables determine the branch but the ANALOG variable is set before the operation begins. It is therefore guaranteed to be stable and only one variable exists that can change. It has been determined that any flashing that may occur in the outputs is not critical.

From the next state maps it can be seen that due to the map-entered variables and the multiple loopings that are necessary to cover the maps, a multiplexer implementation of the next state decoder will simplify the hardware requirements. The schematics for the main controller are shown in Figures 11, 12 and 13.

GPIB Handshake Subcontroller

The GPIB handshake subcontroller is a four-state machine designed to interface to the General Purpose Interface Bus (GPIB) of the 4924 Digital Tape Recorder. Other controllers and subcontrollers use the initiation scheme to interface to this subcontroller. Users of this scheme assume that the GPIB handshake subcontroller is fast enough to transfer data to the 4924 at their fastest rate. The Tektronix® GPIB is an implementation of IEEE Standard 488-1975. This is an interface standard developed to define an interconnection between devices which is independent of the device. The standard is intended not only for use in the devices within one company, but also for compatability of devices that are not manufactured by the same company.

In order to interface to the 4924 only the three handshake lines (DAV, NRFD, and NDAC) and the eight parallel data lines need be used since the 4924 has an off-line LISTEN mode which allows it to accept data under control of these three handshake lines. For the application in this report, the interface system transmits data to the 4924. The interface is therefore the TALKER and the 4924 is the LISTENER. Appendix B contains flow charts and a timing diagram illustrating the operating sequence of the three handshake lines.

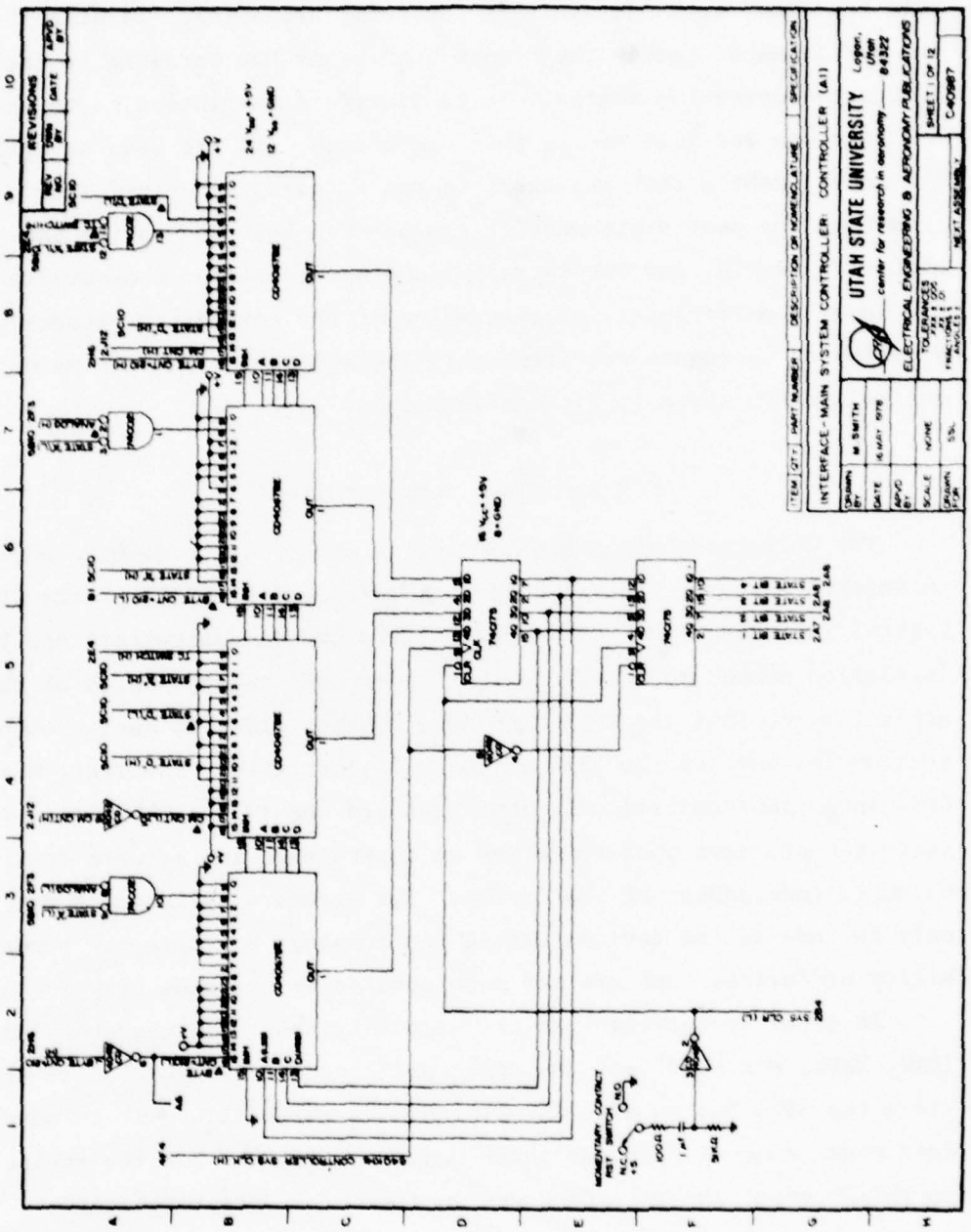


Figure 11. Main System Controller: Schematics (A)

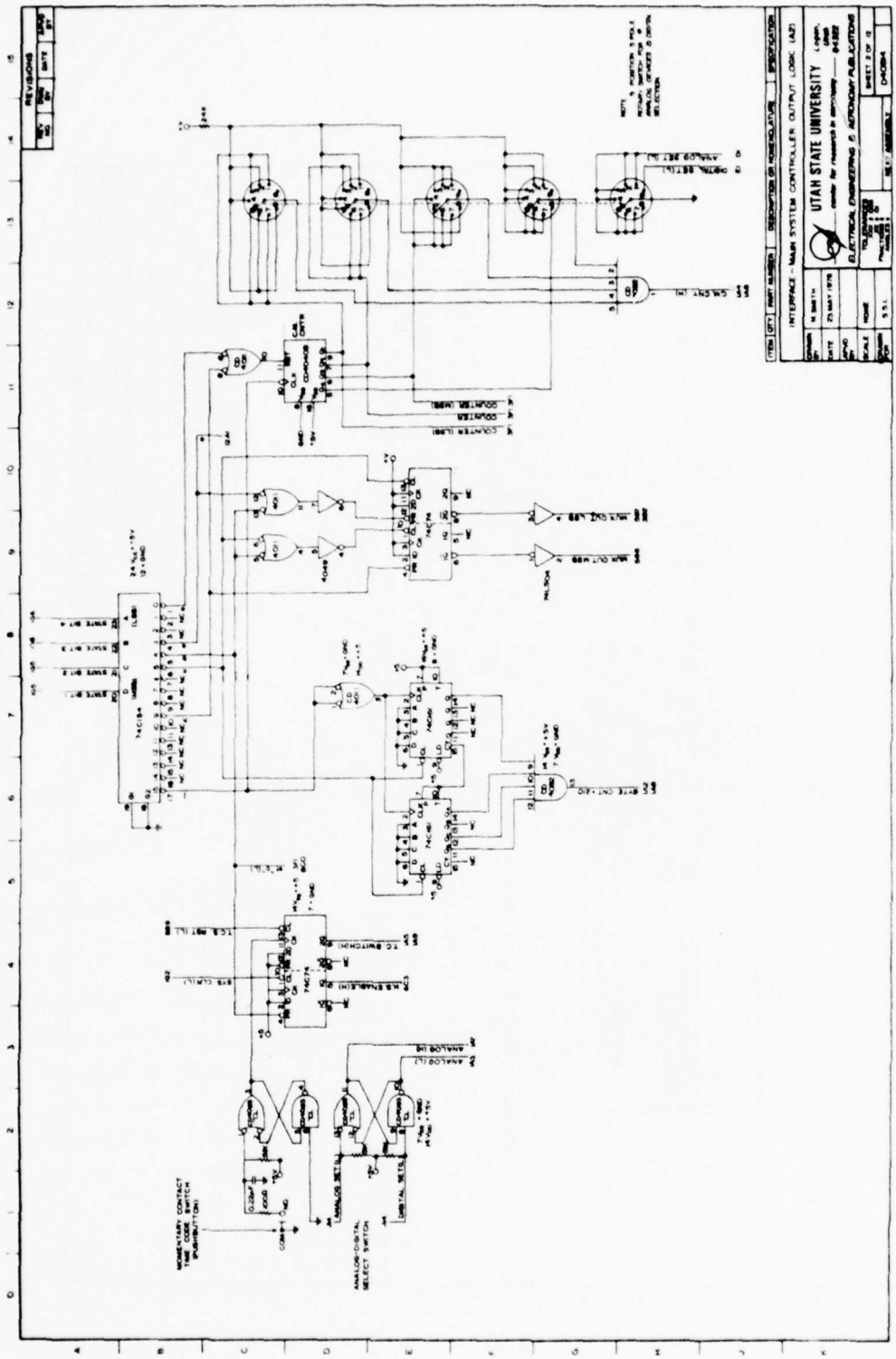


Figure 11. Main System Controller: Schematics (A)

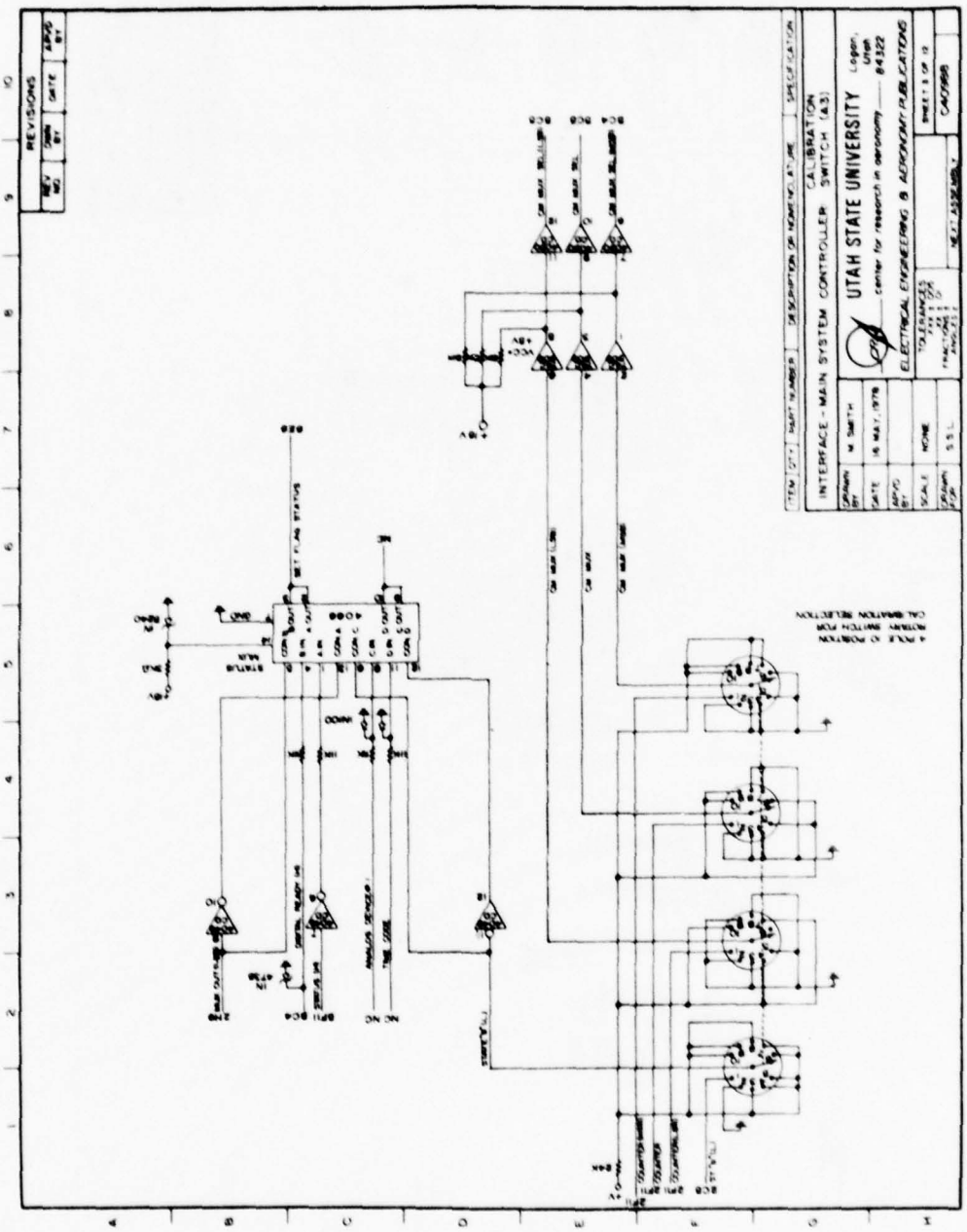


Figure 11. Main System Controller: Schematics (A)

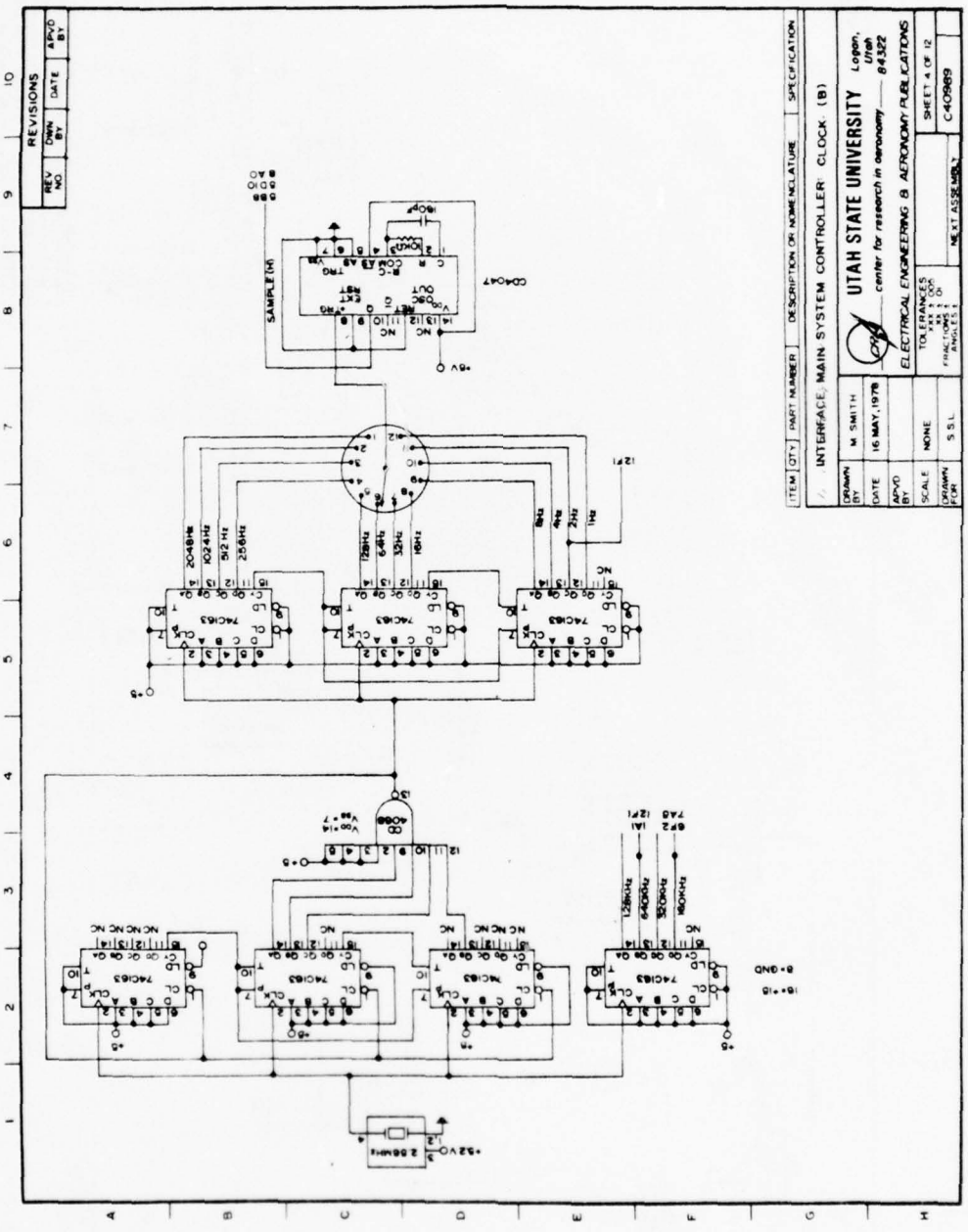


Figure 12. Main System Controller: Schematics (B)

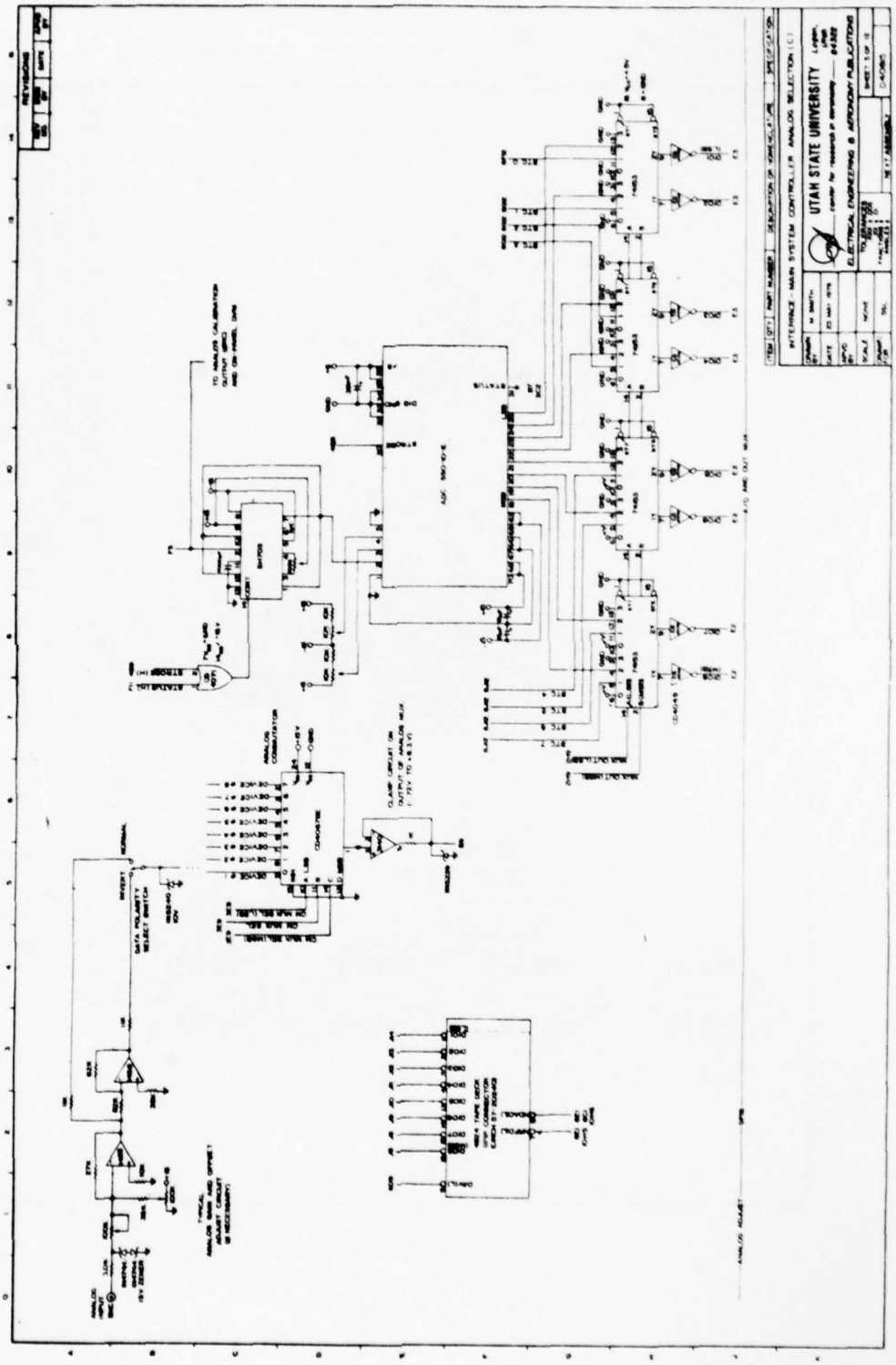


Figure 13. Main System Controller: Schematics (C)

Detailed Operational Description

The flow chart of the GPIB handshake subcontroller is shown in Figure 14. The subcontroller is initialized to state "A" by either a power-up reset or an external reset. In this state the DAV Flag is reset. The Tektronix^{R} GPIB uses negative logic or asserted low logic so that when the DAV Flag is reset it is at the high voltage state. With the exception of the initial time through this routine, state "A" implies that the data has been received by the GPIB device and changes can be made on the data bus. The subcontroller waits in this state until the GPIB device asserts the NDAC line or in other words the line goes to the low voltage state. When this occurs the subcontroller goes to state "B" where the STATUS FLAG is reset. STATUS FLAG is a flag that is set by either the analog routine through the sample rate clock, or the digital data subcontroller and time code subcontroller through the DIGITAL READY signal. It signifies that the analog or digital data is ready to be recorded. The subcontroller remains in this state until the GPIB device deasserts NRFD signifying it is ready for data. The subcontroller proceeds to state "C" to wait for the STATUS FLAG to be set by another subcontroller. When this flag is set, the subcontroller advances to state "D" where the DAV Flag is set to signal the GPIB device that the data on the bus is valid and ready to be recorded. When the data is accepted by the GPIB device, this subcontroller returns to state "A" to re-execute its routine. It should be noted that the subcontroller must wait for NDAC to be asserted in state "B" and deasserted in state "D" to insure the proper operating sequence of the handshake routine.

Implementation

The MDS diagram, the state assignment map, and the NEXT STATE maps are shown in Figure 15. A timing diagram is shown in Figure 16 with some of the analog data routine's information. Using D type flip-flops as the present state holding register, the input decoding logic can be easily implemented with combinational logic. A decoder is used for the output decoder. All state assignments are unit distance to eliminate flashing on the output decoder. The schematic

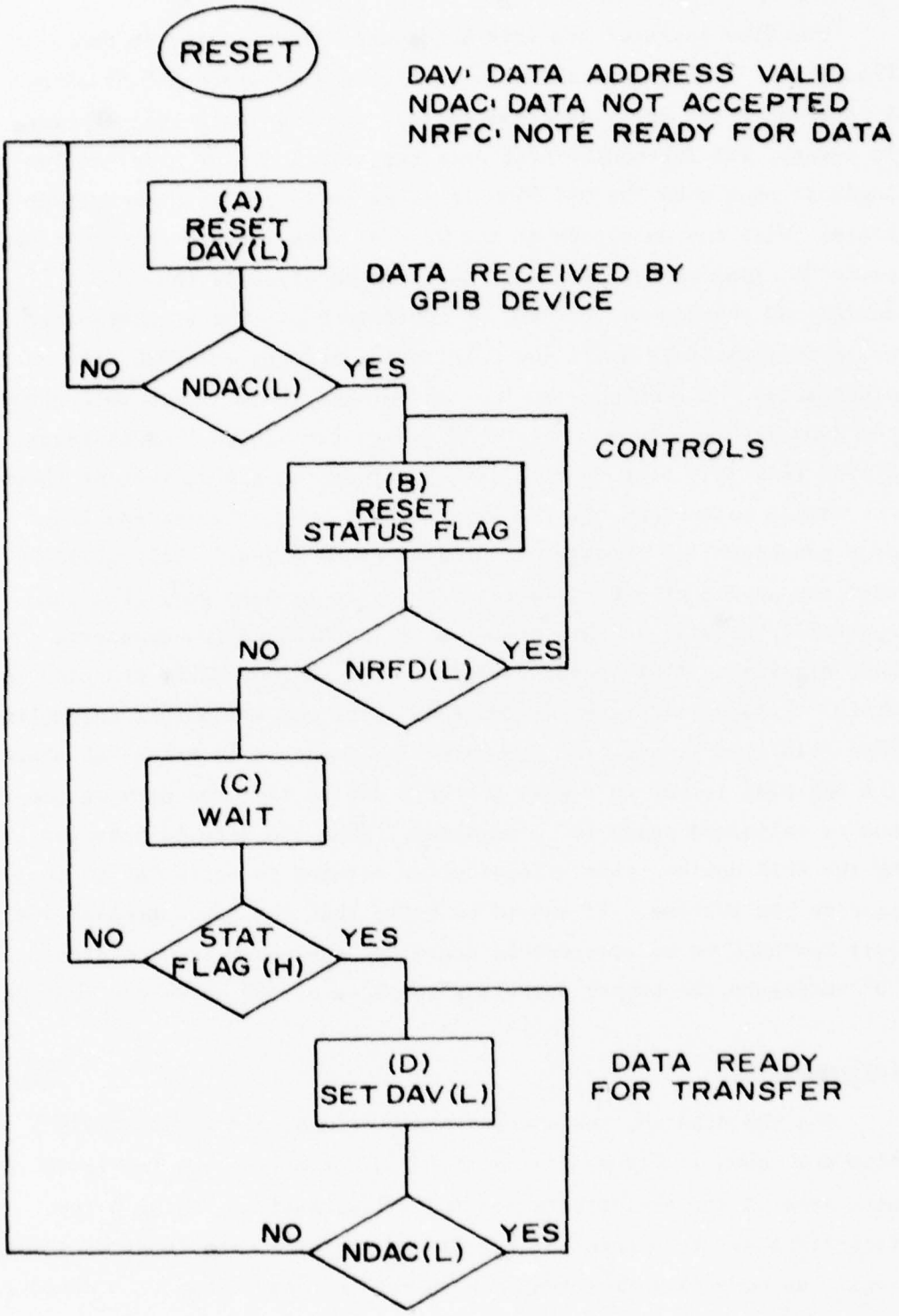


Figure 14. GPIB Handshake Subcontroller: Flow Chart

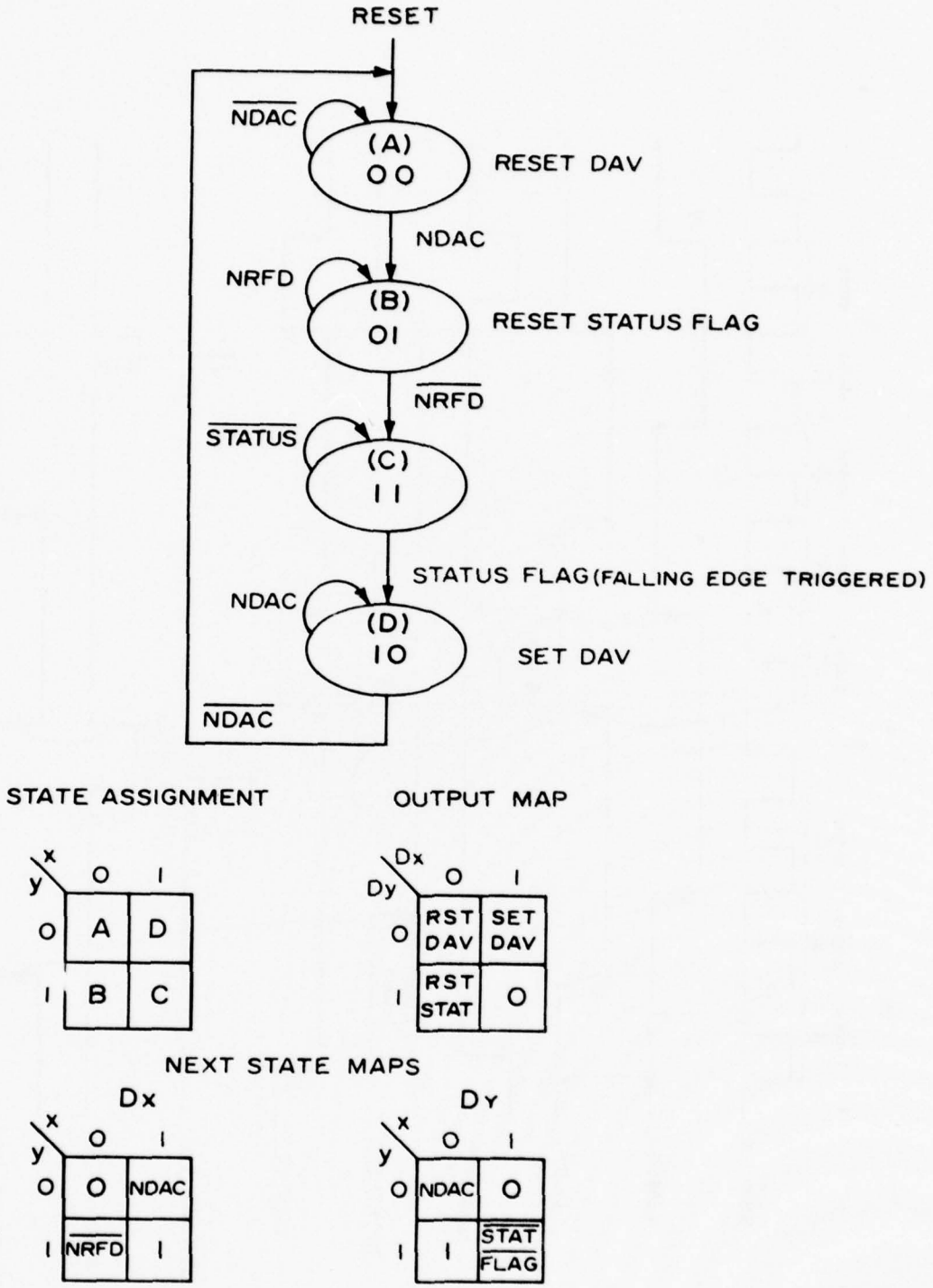


Figure 15. GPIB Handshake Subcontroller: MDS Diagram, State Assignment Map and NEXT STATE Maps

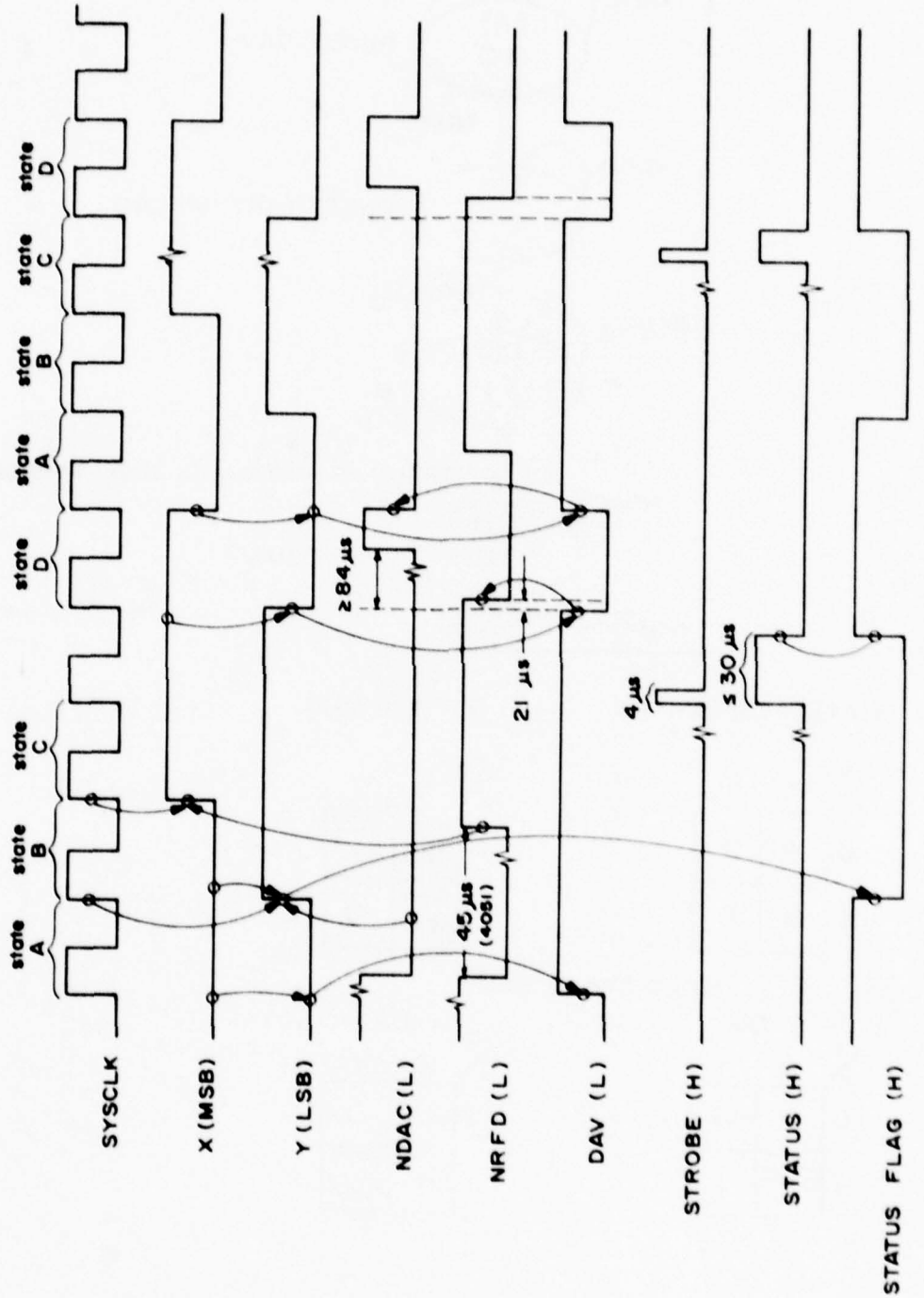


Figure 16. GPIB Handshake Subcontroller: Timing Diagram

for this subcontroller is shown in Figure 17. This subcontroller will transfer data to the 4924 at least 1024 bytes per second, but not constantly at 2048 bytes per second. This is a limitation of the 4924 and not the subcontroller. The 4924 uses a double buffer system to store data before recording it onto the tape. Each buffer holds 256 bytes of data. When one buffer is full, data is stored in the other buffer while the first buffer transfers its data to the tape. When operating at 2048 samples per second, the first buffer has not transferred all of its data to tape by the time the second buffer is full; therefore, only the first 512 samples are recorded at real time.

IRIG Time Code Decoder and Subcontroller

In order for data to be useful, the time during the flight that the data was recorded must be known. Initially an undetected IRIG time code available at the locations where the experimental rockets were launched was recorded onto the tape as a single analog channel. This method required at least 500 bytes of tape space and the user had to visually decode this data to determine the time. This method was subsequently replaced with this IRIG time code decoder and subcontroller.

Operational Overview

The functional partition of this section is shown in Figure 18. The decoder accepts IRIG format B time code with a data rate of 100 parts per second in a BCD format either with a 1 kHz AM carrier or without a carrier. More detailed information of this format is given in Appendix C. The decoder detects the bit type (INDEX MARKER, CODE DIGIT, or POSITION IDENTIFIER) and formats the time code in hours, minutes, and seconds. It then latches this data in a 24 bit latch whose output is available to the front panel display and the IRIG time code subcontroller. The subcontroller interfaces to the main controller by using a handshake scheme. When the handshake to the subcontroller is initiated, the subcontroller uses an initiation scheme to interface to the GPIB handshake subcontroller and transfer the data to the 4924 in three bytes. The subcontroller then finishes the handshake with the main controller.

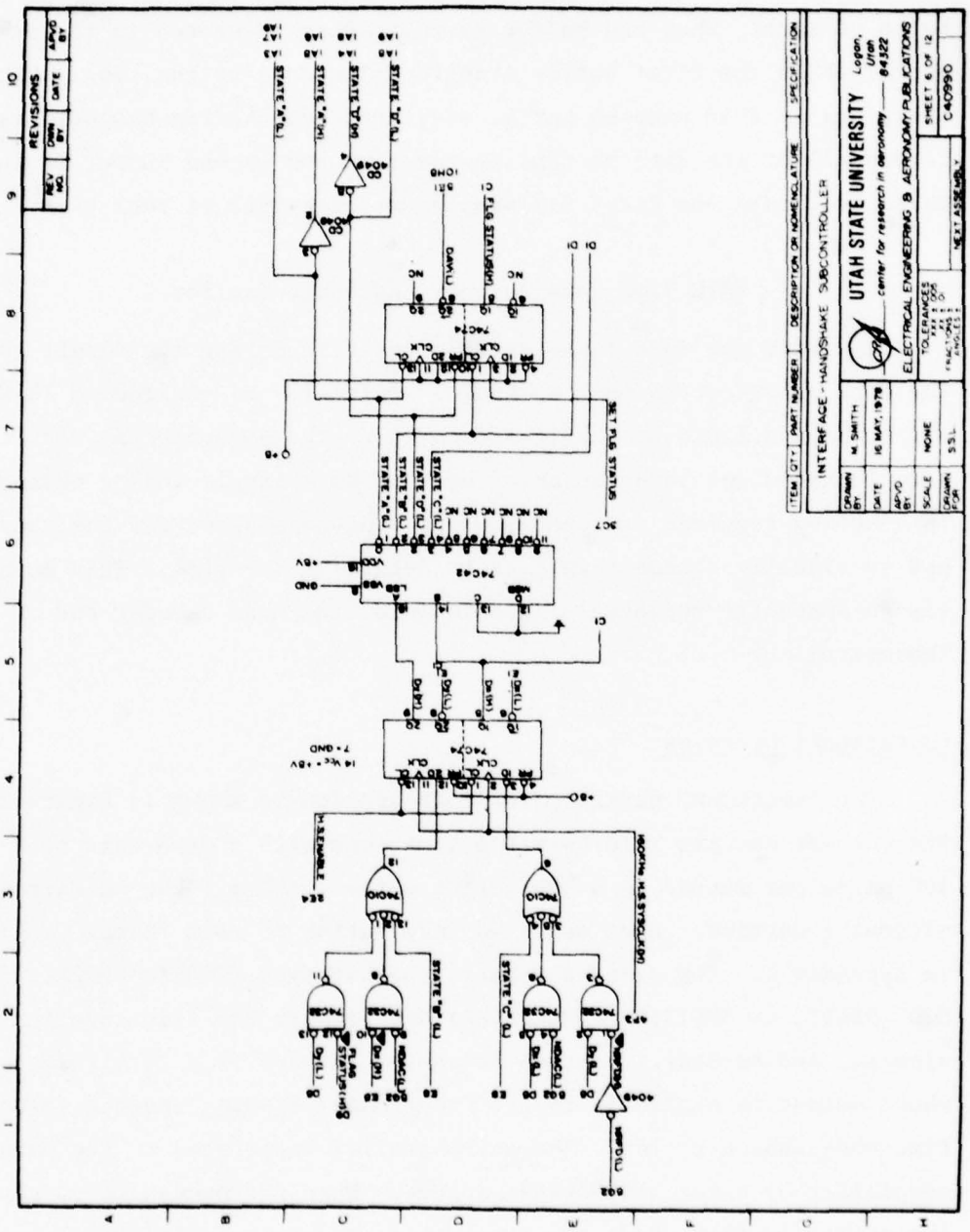


Figure 17. GPIB Handshake Subcontroller: Schematics

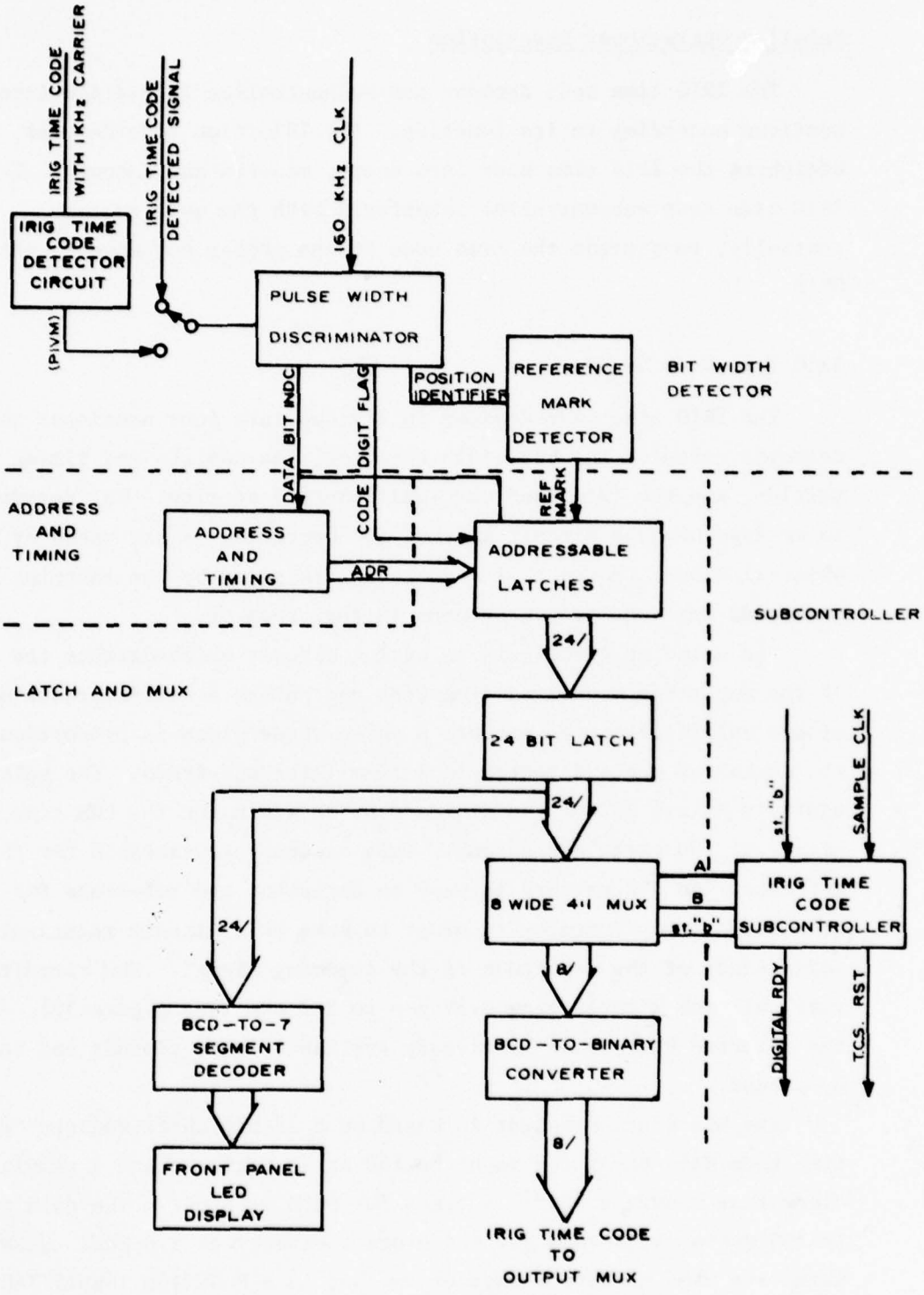


Figure 18. IRIG Time Code Decoder and Subcontroller: Functional Partition

Detailed Operational Description

The IRIG time code decoder and subcontroller is divided into two sections according to its function. The IRIG time code decoder deciphers the IRIG time code into hours, minutes and seconds. The IRIG time code subcontroller interfaces with the main system controller to provide the time code in the proper sequence to the GPIB.

IRIG Time Code Decoder

The IRIG time code decoder is divided into four sections: the detector circuit, the bit width detector, the address and timing section, and the latch and mux (multiplexer) section. The decoder is an asynchronous circuit in that its operation is not paced by an external clock. However, its operation is paced by the incoming time code data and is synchronous in that respect.

The detector circuit is an analog circuit which detects the peaks of the amplitude modulated time code and pulses a retriggerable monostable multivibrator to produce a pulse whose width is proportioned to the number of peaks detected in a 10-millisecond frame. The pulse width is within 20% of the standard pulse width for the PWM time code signal at 100 parts per second. This accuracy is suitable for the detector. An R-C network is used to determine the reference for the peak detecting comparator in order to make this circuit relatively independent of the amplitude of the incoming signal. The circuit works very well for signals from 0.5V p-p to 26V p-p (see Figure 19). If the detected PWM signal is already available, this circuit can be by-passed.

The bit width detector is based on a 17-bit shift register with the time code data being the input to the shift register and a sampling clock that causes a shift 16 times for each data bit. The data rate is 100 parts per second and the clock frequency is 1.6 kHz. NAND gates are used to detect whether the bit is a POSITION IDENTIFIER, CODE DIGIT, or INDEX MARKER by the number of consecutive "high" bits in the 17-bit shift register. The detection format in Table 1 is used. The detection range is extended past the standard width to compensate

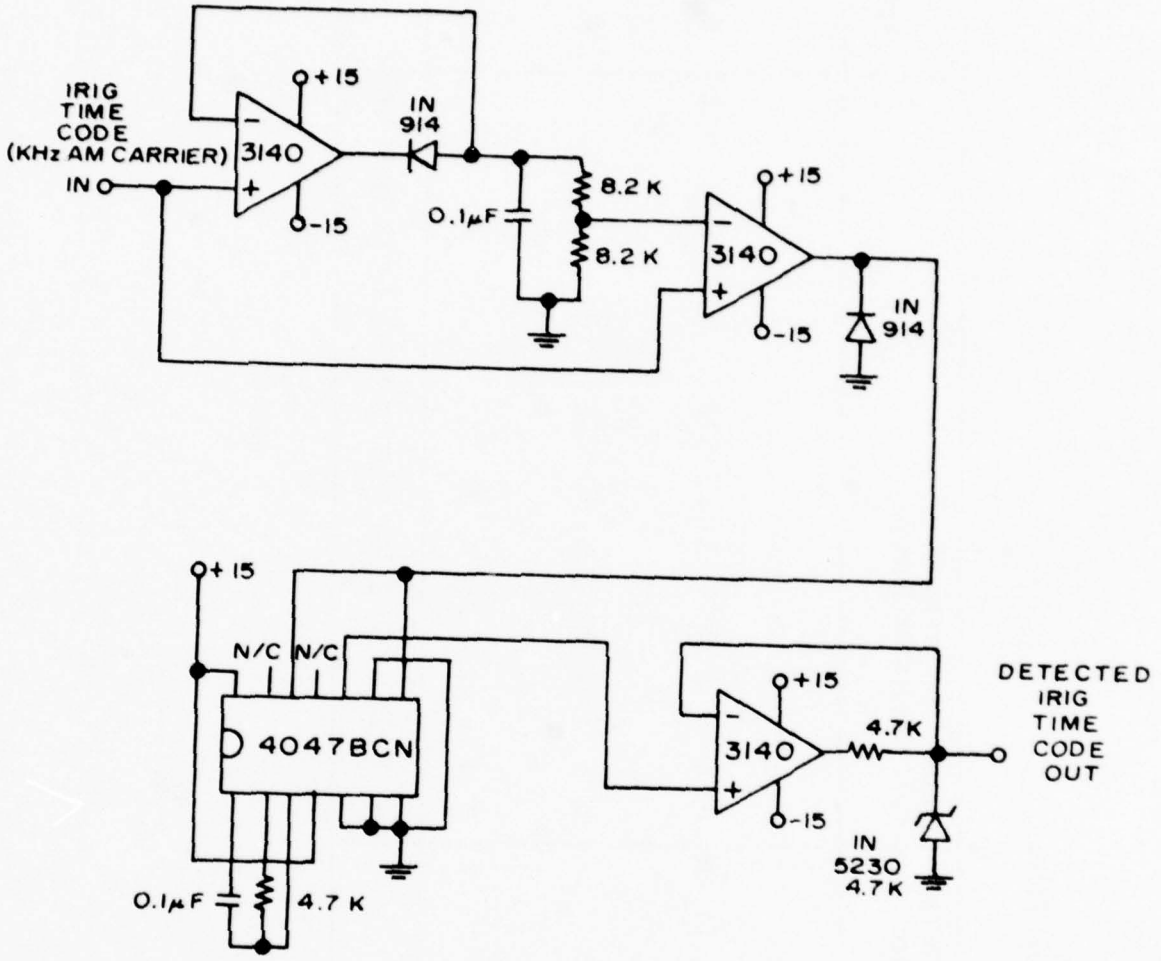


Figure 19. IRIG Time Code Detector Circuit

TABLE 1: IRIG Time Code Detection Format

	Number of "high" Bits Detected	Detection Format of Shift Register Output	tpw Range (msec)
POSITION IDENTIFIER or REFERENCE MARKER (8 msec)	11, 12, 13, 14, 15	0 ϕ ϕ ϕ 1 1 1 ϕ 1 ϕ 1 ϕ 1 ϕ ϕ ϕ 0	6.87 to 9.375
CODE DIGIT Logic "1" (5 msec)	7, 8, 9, 10	0 ϕ ϕ 1 1 1 ϕ 1 1 1 ϕ 0	4.375 to 6.25
INDEX MARKER Logic "0" (2 msec)	3, 4, 5, 6	0 ϕ ϕ 1 1 ϕ ϕ 0	1.875 to 3.75
		0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	

for the inaccuracy of the carrier blanking circuit.

The address and timing section consists of a counter, a monostable multivibrator, and a demultiplexer. The counter forms the address of location where the data bit is to be latched and counts the number of data bits. The monostable multivibrator pulses the demultiplexer which enables the addressed latch to write ($\overline{WD}$) the data. A flag, BIT CNTR=24, is set when all data bits have been latched.

The latch and mux section consists of a 24-bit addressable latch, a 24-bit latch, an 9 wide 4 to 1 mux, and an 8-bit BCD-to-binary decoder. The 24-bit addressable latch is used to hold the data, bit by bit as new data enters. When all 24 bits are updated, the 24-bit latch is used as a holding register. The outputs of this latch go to a front panel display and to the 8 wide 4 to 1 mux used to output the data in hours, minutes, and seconds in 8-bit bytes. The data is then converted from BCD to binary and sent to the output mux of both the analog data circuit and the digital data circuit for their use.

Further explanation of the operation of the IRIG time code decoder as a whole is described in the flow chart and timing diagram in Figure 20. With either a power-up reset or an external reset, the 17-bit shift register is cleared and the bit counter, time code (T.C.) switch, and REFERENCE MARKER FLAG are reset. When the REFERENCE MARKER FLAG is set, by the bit width detector seeing two consecutive position identifiers the clock to the bit counter is enabled. This clock is an OR function of the CODE DIGIT DETECTOR and the INDEX MARKER DETECTOR. It is called the DATA BIT INDICATOR. On the rising edge of the DATA BIT INDICATOR the CODE DIGIT FLAG is reset and the WRITE DISABLE (WD) line to the appropriate addressable latch is pulsed with a negative going pulse whose rising edge latches a "1" if the CODE DIGIT FLAG has been set by the code digit detector, or a "0" if the CODE DIGIT FLAG has not been set. On the falling edge of the DATA BIT INDICATOR the bit counter is incremented. The time code is latched one bit at a time until the bit counter equals 24, at which time all of the time code that is needed has been latched. The REFERENCE MARKER FLAG is the reset along with the bit counter. If the main controller is not requesting the time code (state "b"), the new time code is clocked into the 24-bit latch. The output of this latch goes to a BCD-to-7 segment

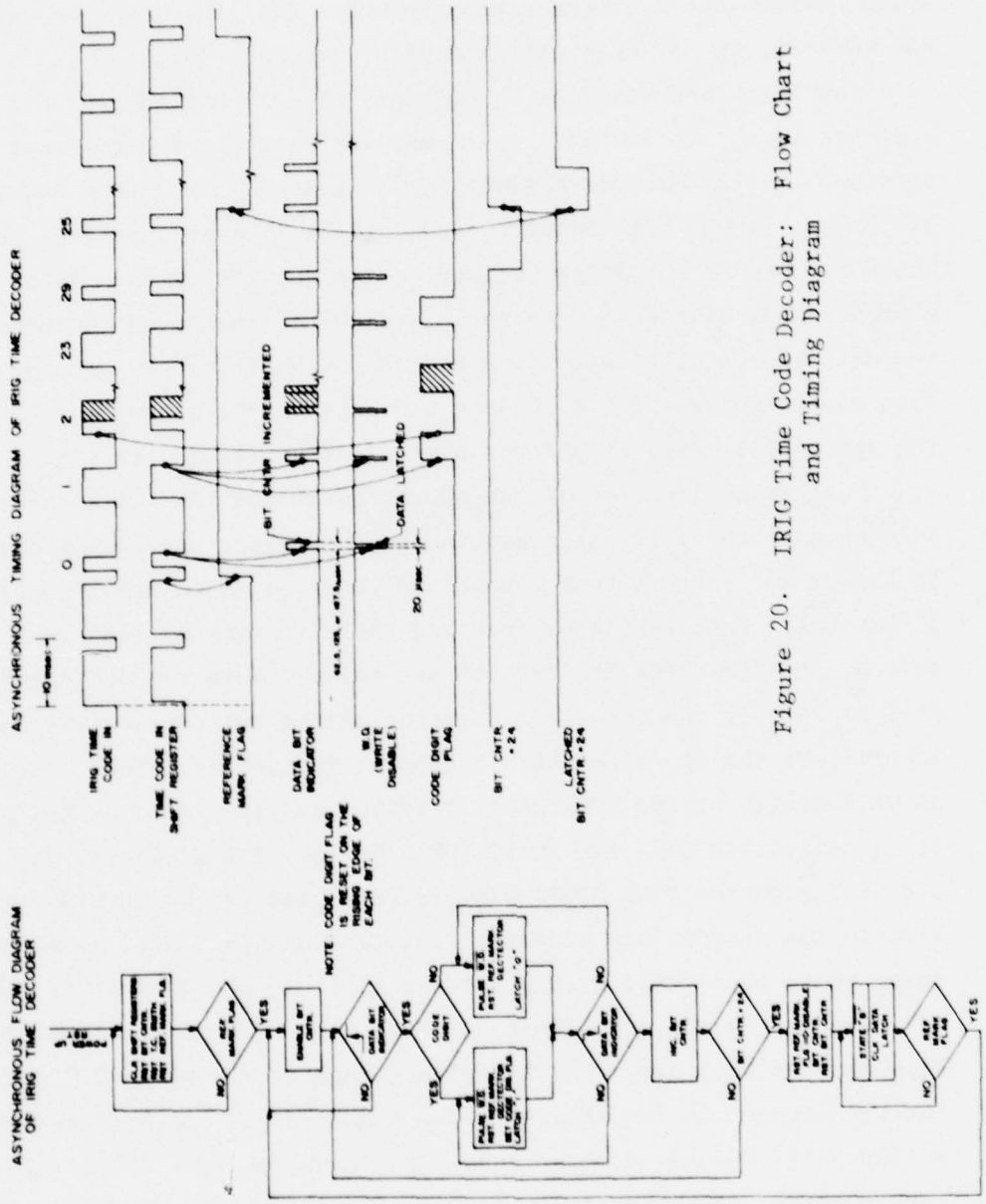


Figure 20. IRIG Time Code Decoder: Flow Chart and Timing Diagram

decoder, which in turn goes to a front panel display and to the IRIG time code subcontroller's 8 wide 4 to 1 mux. The decoder then waits for the next REFERENCE MARKER FLAG to restart its serial time code data latching routine. This updating occurs once each second.

IRIG Time Code Subcontroller

The IRIG time code subcontroller's operation is shown in the flow chart and timing diagram in Figure 21. The sample rate clock of the analog routine is the system clock for this subcontroller. The subcontroller is reset when the main controller is not in state "b" and the multiplexer (mux) counter is reset. When the main controller enters state "b" it initiates the handshake interface scheme to this subcontroller. The mux counter is enabled on the next rising edge of the sample clock and DIGITAL READY (RDY) is sent to the GPIB handshake subcontroller as the signal for the initiation interface scheme and also to signify that the digital time code data is valid. This data goes through a BCD-to-binary convertor and to the output mux of the main controller. The first data byte is the hours section of the time code. On the next sample clock the mux counter is incremented to the minutes section of the time code and DIGITAL RDY is again issued. The next sample clock increments the mux counter to the seconds section of the time code and issues DIGITAL RDY. T.C. SWITCH is reset as the return handshake signal to the main controller. When the main controller leaves state "b" the IRIG time code subcontroller is reset and cleared.

Implementation

The schematic for the IRIG time code decoder and subcontroller is shown in Figures 22 and 23. An MDS diagram and NEXT STATE maps are not included since a non-traditional design approach was used for the decoder and the circuit was derived from the functional partition. The controller can be implemented simply by using a counter to generate the address for the digital output mux and to count the number of data bytes.

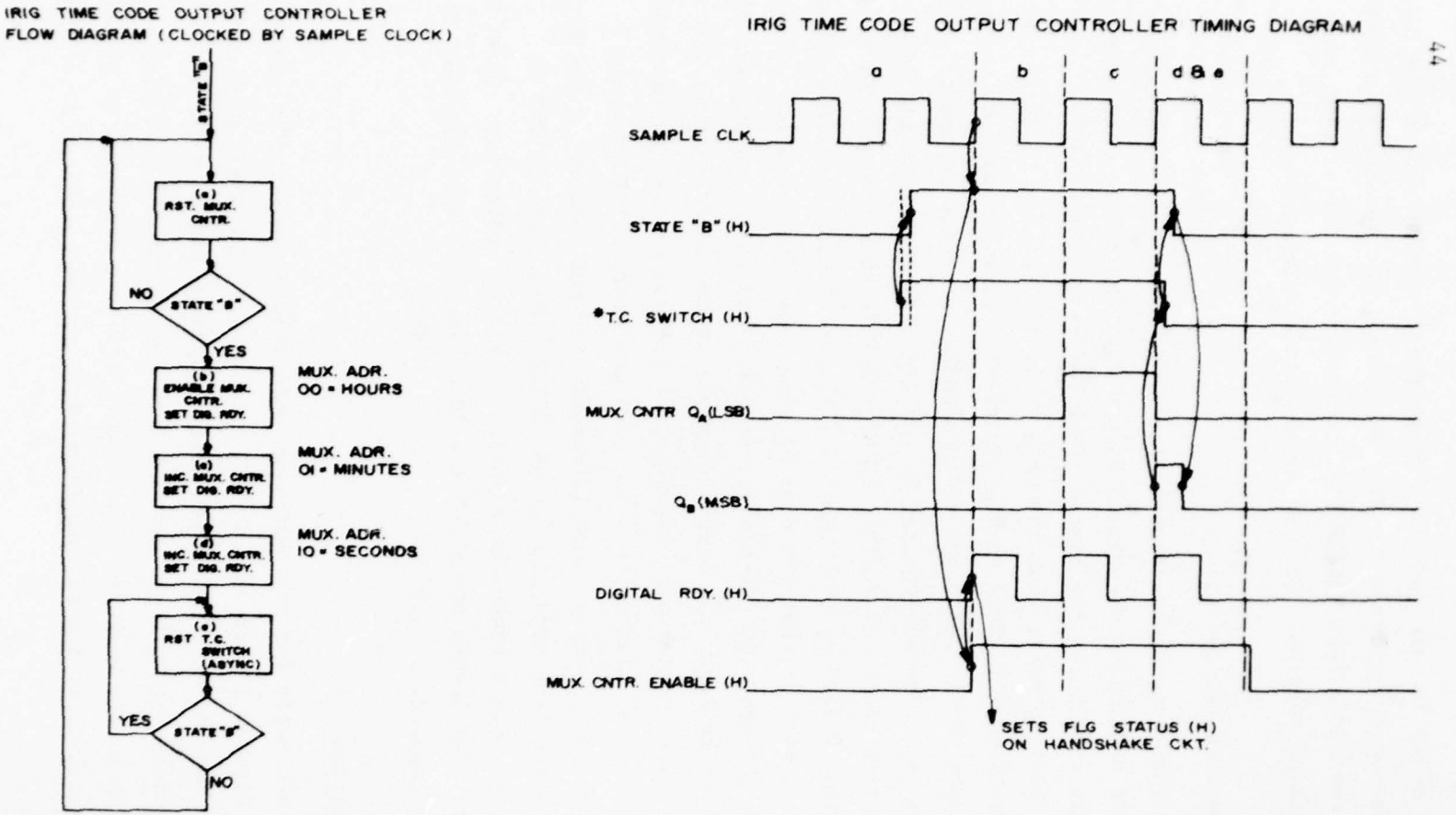


Figure 21. IRIG Time Code Subcontroller: Flow Chart and Timing Diagram

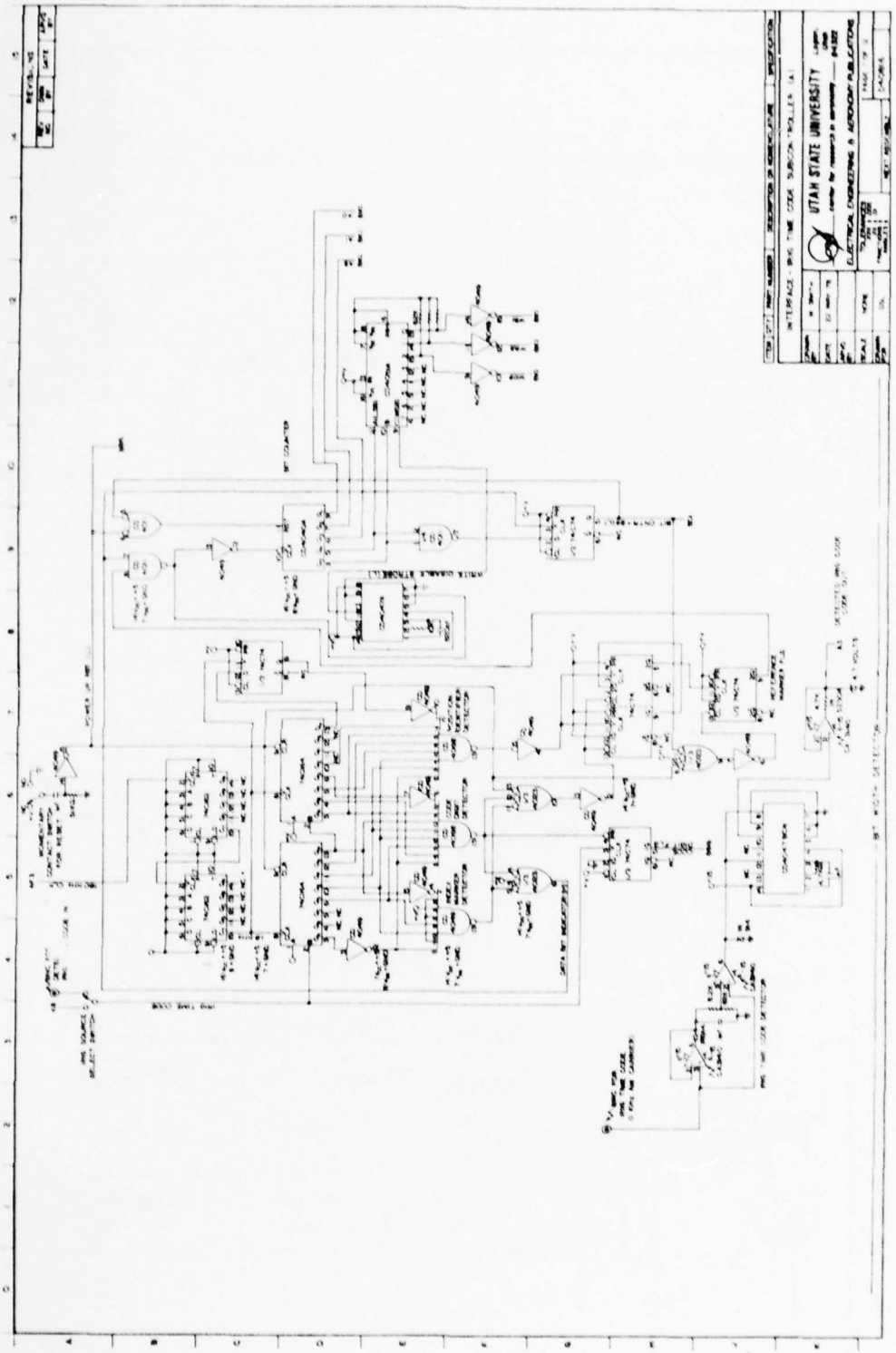


Figure 22. IRIG Time Code Subcontroller: Schematics (A)

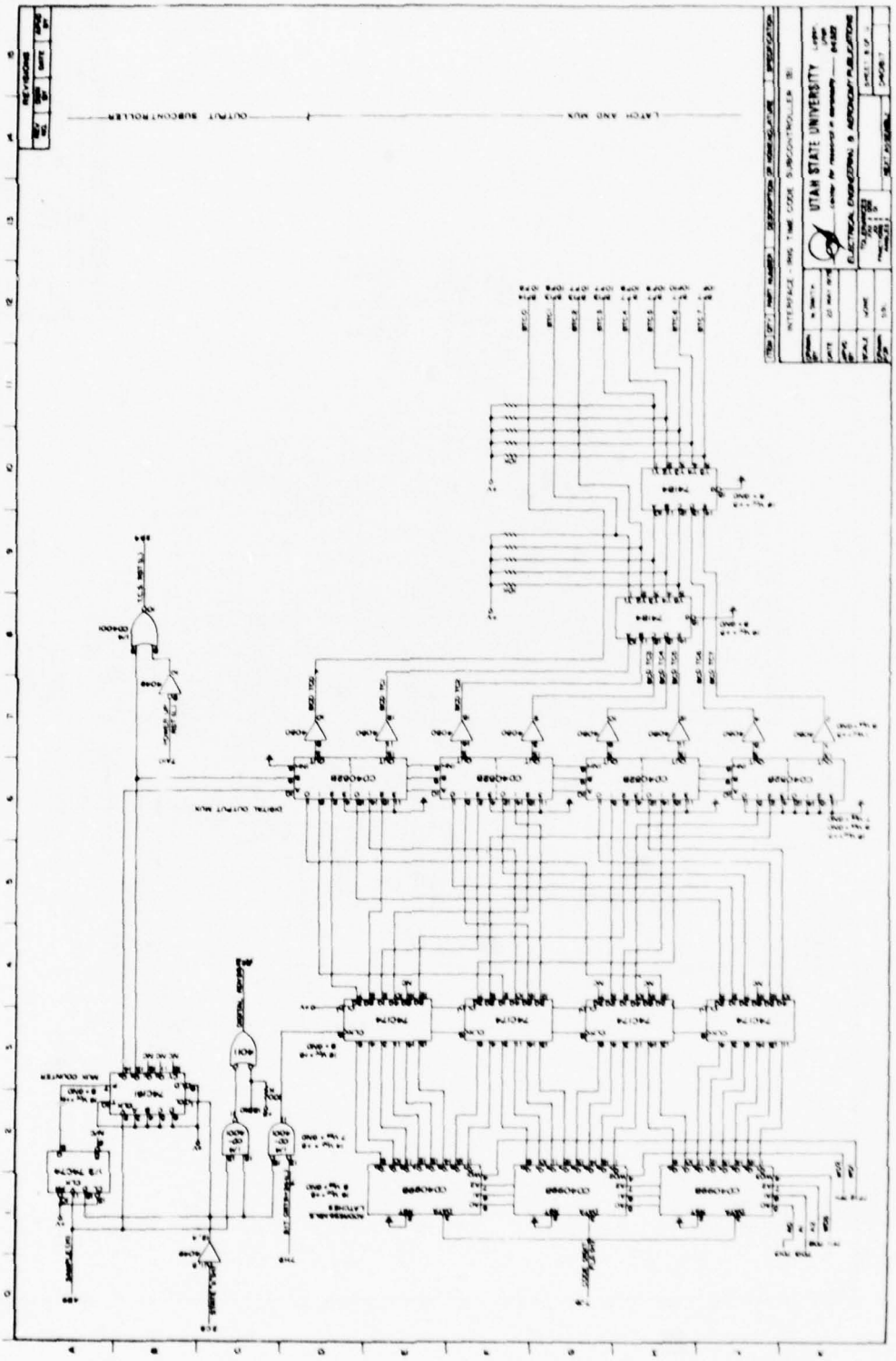


Figure 23. IRIG Time Code Subcontroller: Schematics (B)

Digital Data Subcontroller

The digital data subcontroller accepts a single serial digital data channel, synchronizes itself to the data, and transfers the data in 8-bit bytes to the 4924 Digital Cartridge Tape Drive through the use of the GPIB handshake subcontroller. The serial digital data is transmitted from the experimental instrument at a constant rate with a sync word, a set number of data words, and so on. The sync word is a special binary word that is included in the data in order that the word boundries and data frame boundries can be interpreted. That is, by finding the sync word in a string of serial digital data bits, the data words can be identified or synchronized. As an example, one version of the plasma frequency probe built by the Space Science Laboratory transmits a 16-bit sync word of

0000 0000 0001 1101

and then 31 data words of 15 bits each at 1000 bits per second. Thirty-two words are in the data frame. By locating this in a serial digital data stream, the data words and data frame can be identified.

Operational Overview

The subcontroller is composed of two main sections; a synchronization (sync) detector and the main digital data subcontroller that interfaces to the sync detector using the monitor scheme. A functional partition of this subcontroller is shown in Figure 24. A bit synchronizer circuit is used to generate a clock pulse that occurs when the middle of the serial digital data bit is present. This signal is used to clock the data into a 16-bit latch on the falling edge of each clock pulse. The output of this latch is sent to the sync word detector and an 8-bit latch for holding the GPIB destined data. The sync word detector has a set of 16 double-pole, double-throw, 3-position switches configured to allow the user to select a 0 (low state), ϕ (don't care state), or 1 (high state) for each bit of the sync word. An output from the sync word detector, SYNC WORD, signals the sync detector that the sync word is present in the 16-bit

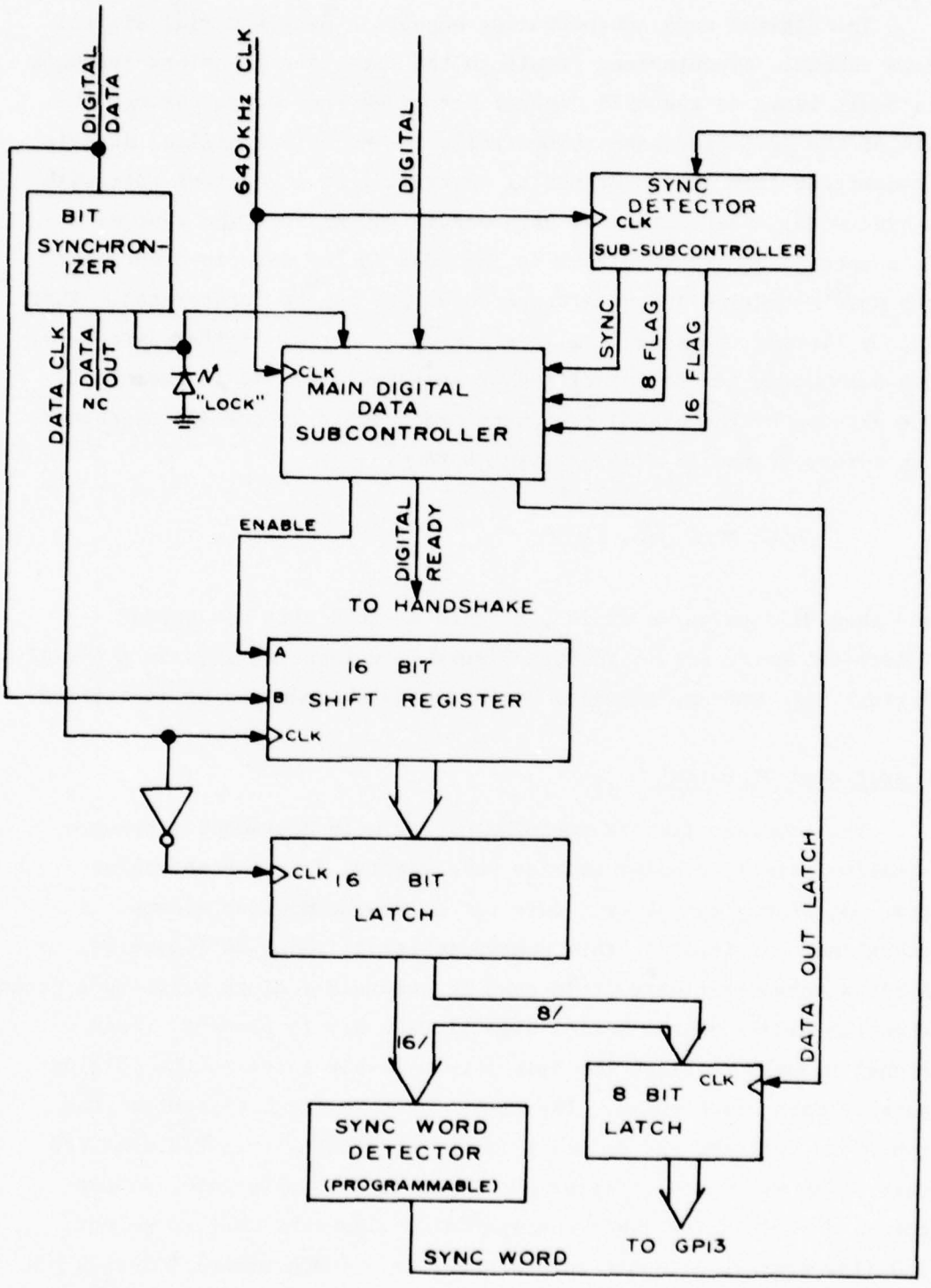


Figure 24. Digital Data Subcontroller: Functional Partition

latch. A double thumbwheel switch allows the user to set the total number of 16-bit words in a data frame. The sync detector synchronizes itself to the digital data by waiting for the sync word, counting selected number of 16-bit data words in a data frame, and then checking to see if the sync word is present again. This method greatly reduces the possibility of mistaking a data word, that has the same format as the sync word, for the sync word. If the second sync word is present, the main digital data subcontroller is issued SYNC as part of the monitor interface scheme. The main digital data subcontroller then begins to transfer the digital data in 8-bit bytes to the 4924 through the GPIB handshake subcontroller. To aid in formatting the data for time determination, a mark (253 binary) is placed on the tape every 4 seconds. This mark has priority over the digital data so that the time determining integrity is preserved. Data after this mark are always begun with the first 8 bytes of the next 16-bit data word. Data are transferred until the current type file is full.

Synchronization Detector Detailed Operational Description

The flow chart in Figure 25 illustrates the operation of the synchronization detector. On a power-up reset or external reset, the detector is initialized to state "t" where the bit counter, word counter, and SYNC FLAG are reset and the clock to SYNC WORD flag is enabled. When SYNC WORD is present the detector circuit goes to state "u" where the bit counter is enabled and SYNC WORD is reset. When the bit counter is equal to 8 the detector advances to state "u". Two outputs conditional on SYNC FLAG are then asserted. That is, the 8 FLAG is set and the digital data is latched into the 8-bit latch if SYNC FLAG is set. Otherwise no output occurs. When the bit counter is equal to 16, state "w" is entered, the bit counter is reset and the word counter is incremented. SET 16 FLAG and DATA LATCH are two outputs conditional on SYNC FLAG in this state. The detector accepts the digital data until the word counter is equal to the front panel setting which implies that the data frame is finished and the next SYNC WORD should be in the 16-bit latch. Therefore, in state "x" the word counter is reset and the flip-flop that

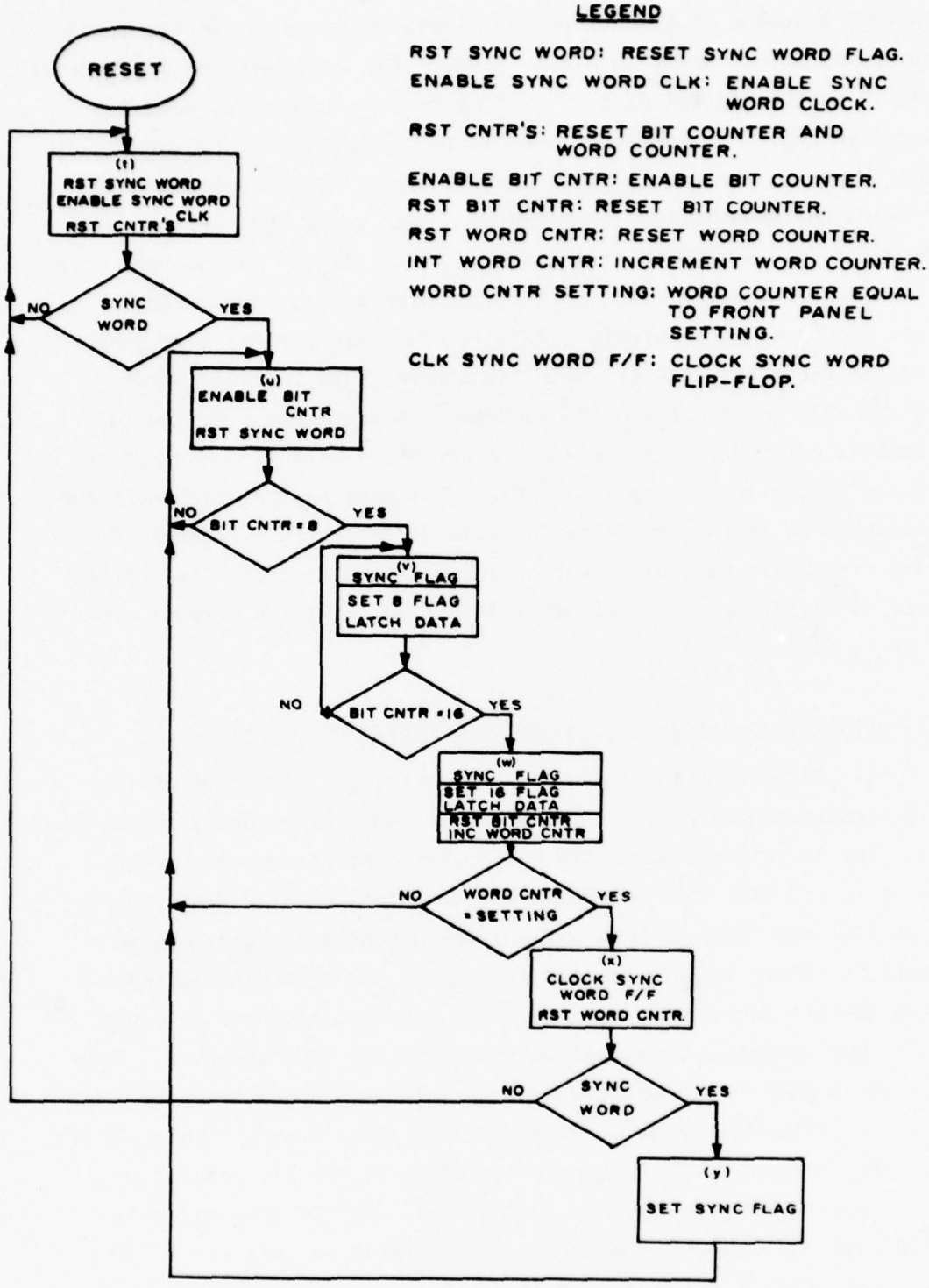


Figure 25. Synchronization Detector: Flow Chart

checks for SYNC WORD is clocked. If the sync word is present, the detector goes to state "y" where SYNC FLAG is set to enable the conditional outputs to signal the main digital data subcontroller. The detector then returns to state "u" to continue its operation. If the sync word is not present, the detector returns to state "t" to look for the sync word. If the sync word is lost during the routine, SYNC WORD is reset and the detector returns to state "t" to resume searching. Three LEDs are on the front panel to indicate to the user when the data is synchronized (DATA SYNC) or not synchronized (NO DATA SYNC) and when the bit synchronizer is locked on the incoming serial digital data (LOCK).

Implementation

The MDS Diagram, state assignment map and NEXT STATE maps are shown in Figures 26 and 27. The technique of using D-type flip-flops as the present state holding register will once again be used. Due to the small number loopings that are possible and the numerous outputs required, multiplexers will be used for the input decoding logic and a decoder will be used as the output decoding logic. Since branching is only done on one asynchronous variable at a time the inputs are not latched. The outputs are latched to prevent flashing since all NEXT STATE state assignments are not unit distance. The schematics are shown in Figures 28, 29 and 30.

Main Digital Data Subcontroller Detailed Operation Description

The main digital data subcontroller's operation is shown in the flow chart in Figure 31. Power-up reset or an external reset starts the subcontroller in state "m" where the 4 SEC flag is reset and the digital output multiplexer is set to select the IRIG time code input. If the main system controller executes the transfer of control interface scheme to this subcontroller by asserting DIGITAL, the subcontroller moves to state "n" and enables the 16-bit shift register of the synchronization detector. It waits in this state for either the 4 SEC flag, which occurs every four seconds as a time determining bench mark, or for a SYNC signal from the sync detector. The 4 SEC

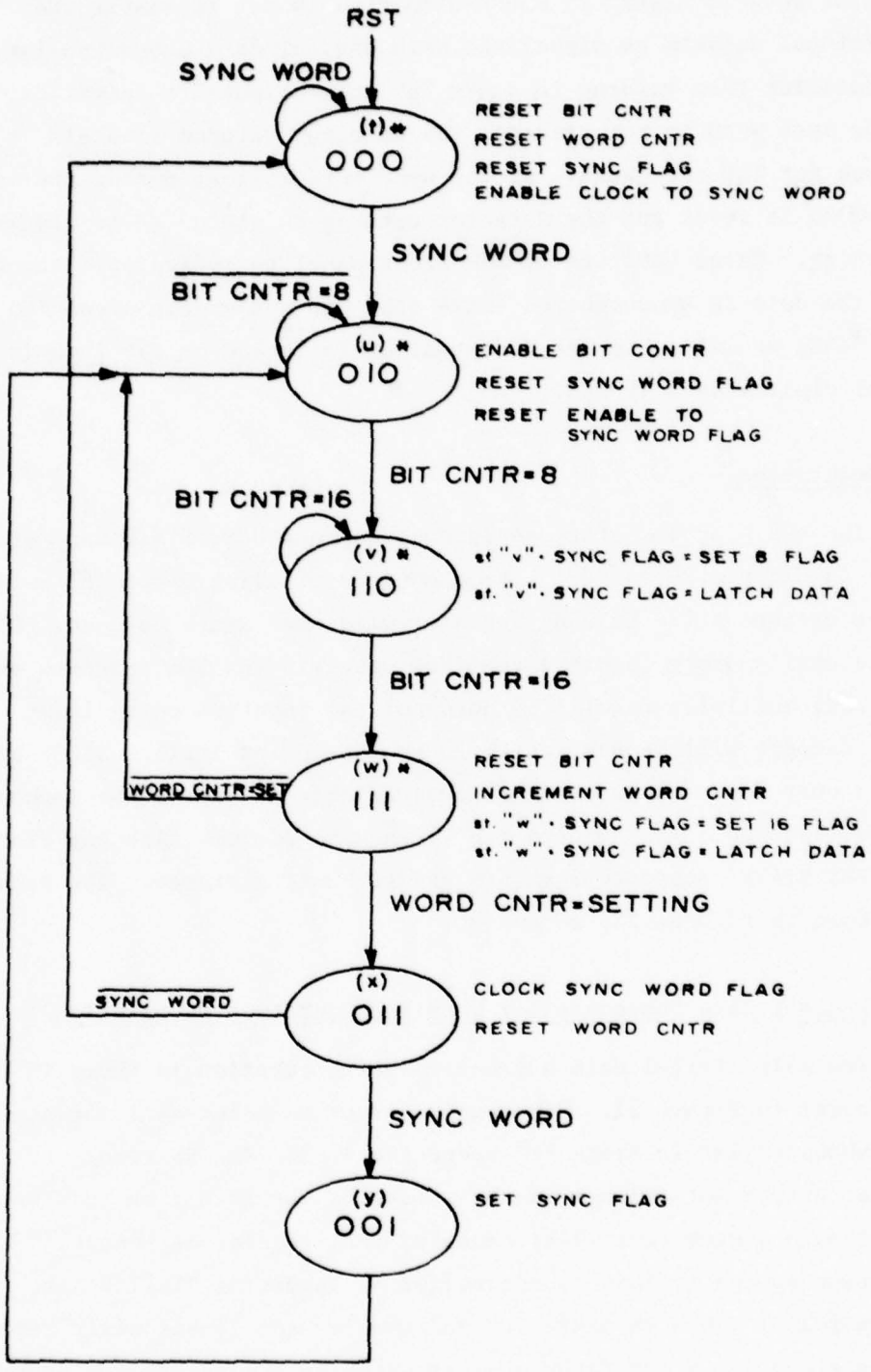


Figure 26. Synchronization Detector: MDS Diagram

STATE ASSIGNMENT

A B / C	00	01	11	10
0	t	u	v	∅
1	y	x	w	∅

NEXT STATE MAPS

D_A (MSB)

A B / C	00	01	11	10
0	0	BIT CNTR = 8	1	0
1	0	0	0	0

D_B

A B / C	00	01	11	10
0	SYNC WORD	1	1	0
1	1	0	1	0

D_C (LSB)

A B / C	00	01	11	10
0	0	0	BIT CNTR = 16	0
1	0	SYNC WORD	WORD CNTR = SET	0

Figure 27. Synchronization Detector: State Assignment and NEXT STATE Maps

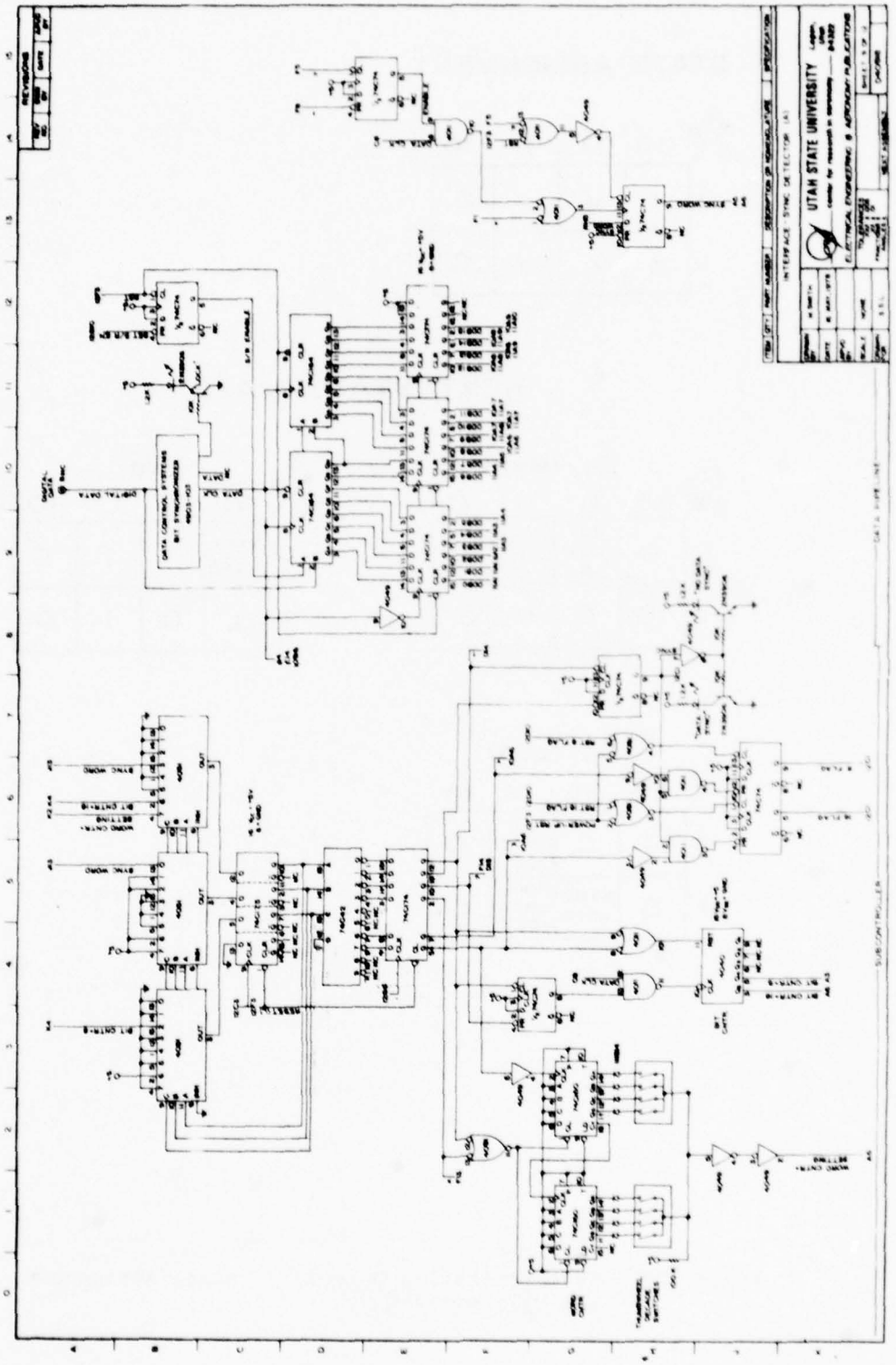


Figure 28. Sync Detector: Schematics (A)

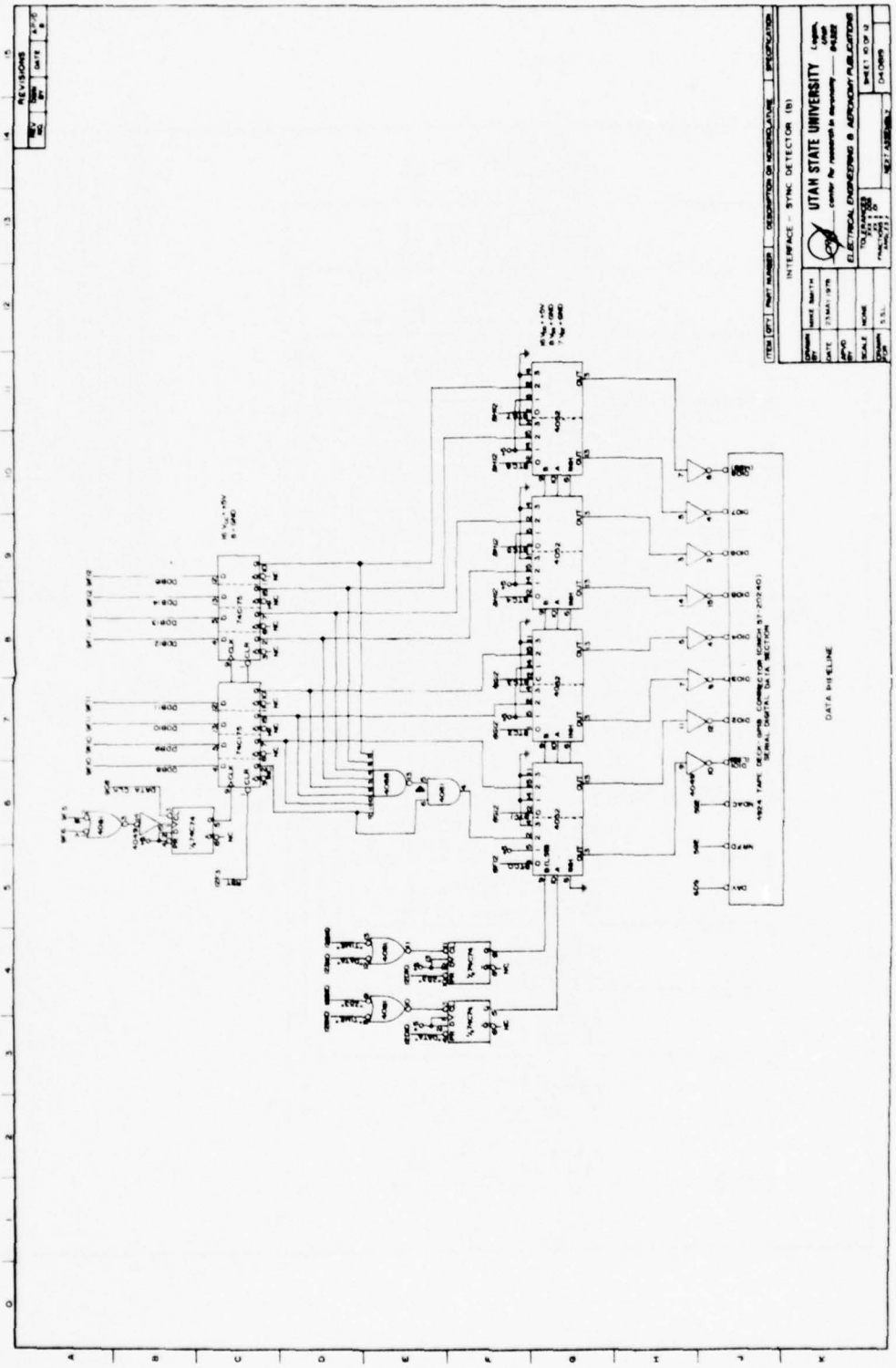


Figure 29. Sync Detector: Schematics (B)

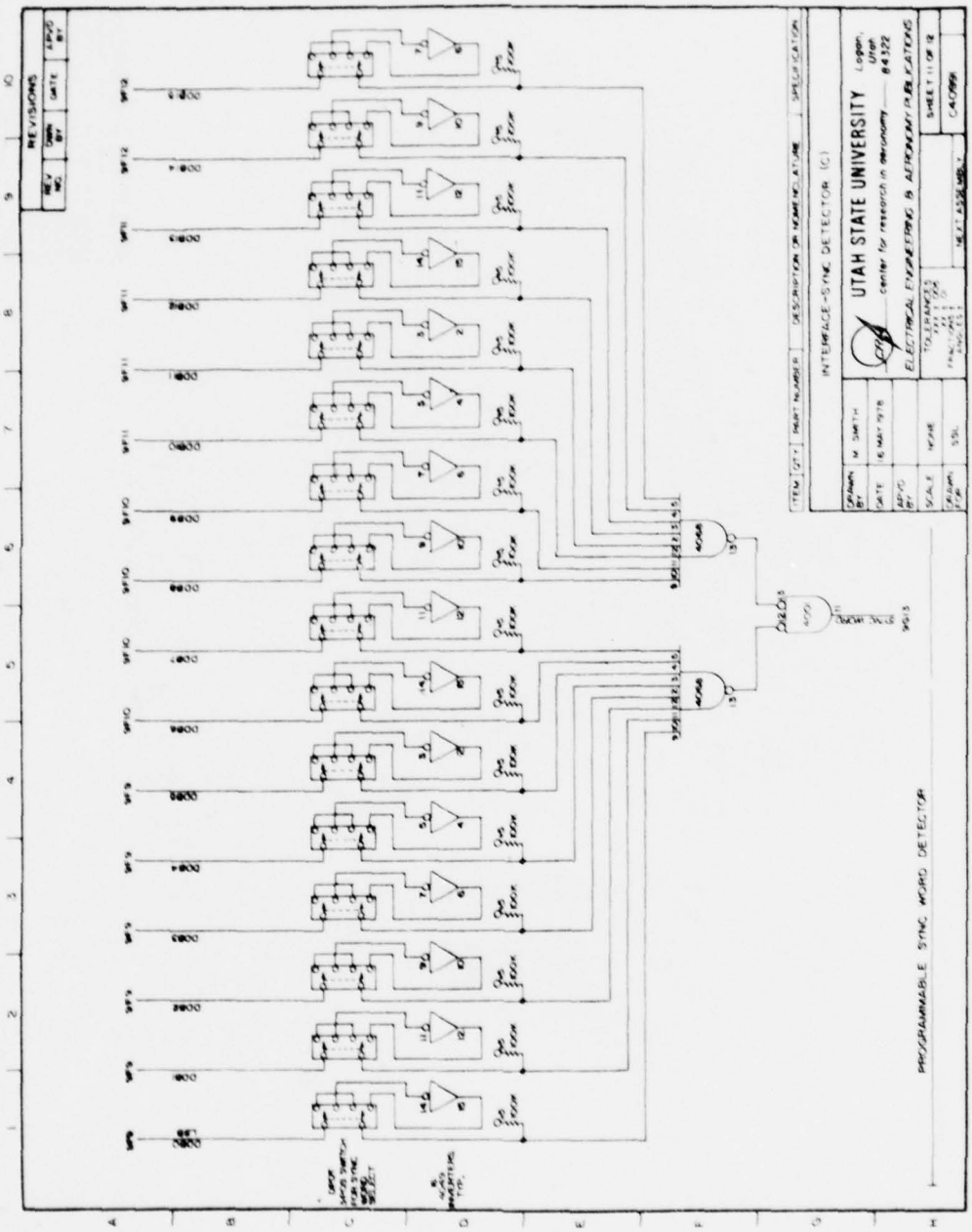


Figure 30. Sync Detector: Schematics (C)

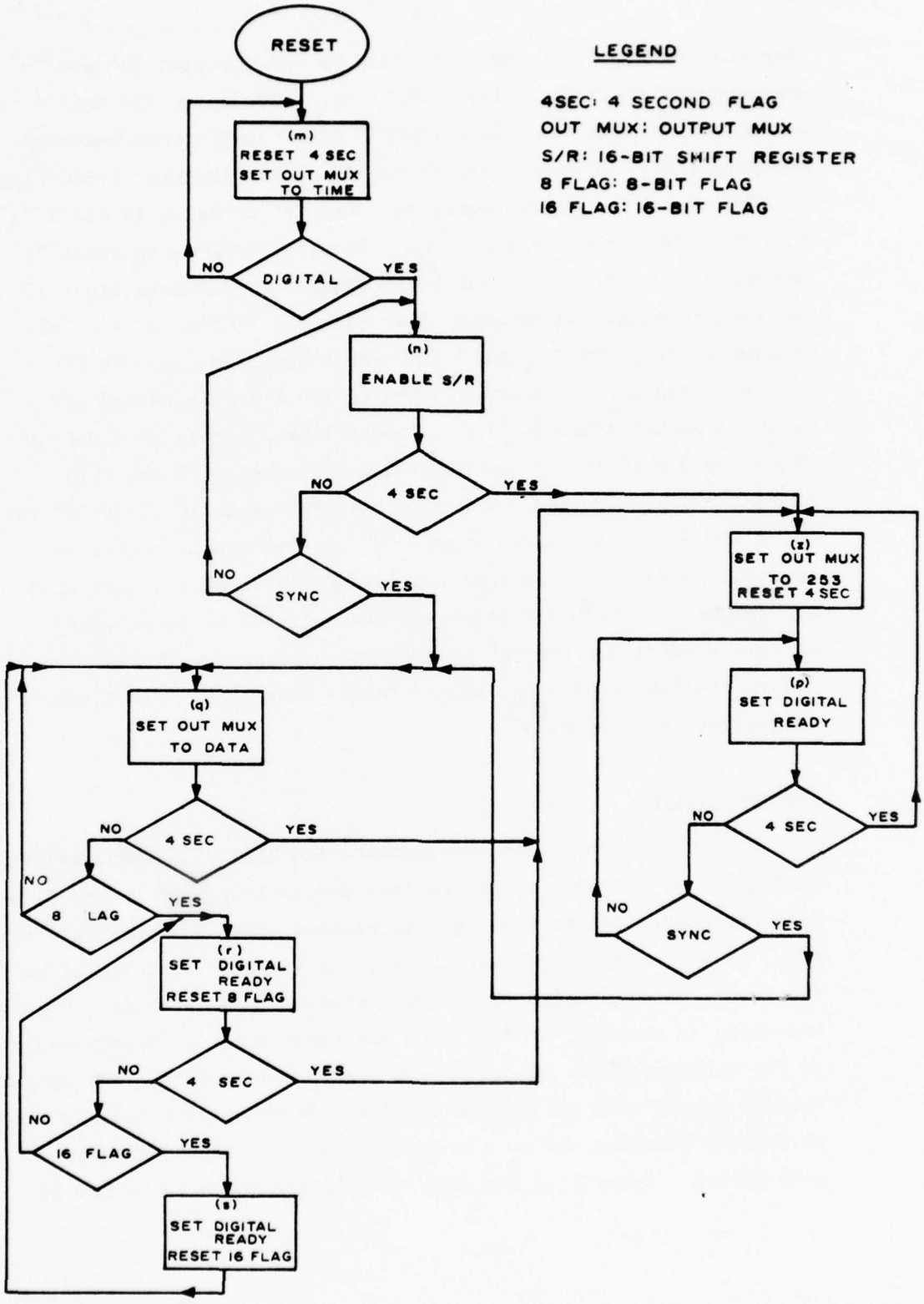


Figure 31. Main Digital Data Subcontroller: Flow Chart

flag has priority. If the 4 SEC flag is seen, states "z" and "p" are executed which reset the 4 SEC flag, selects the 253 mark on the digital output mux and pulses DIGITAL READY to the GPIB handshake subcontroller. It then waits in state "p" for the next 4 SEC flag or SYNC signal before returning to state "z" or going to state "q". When the SYNC signal is seen, the subcontroller goes to state "q" where the digital output mux is set to the 8-bit digital data line. If the 4 SEC flag is seen, the subcontroller executes states "z" and "p". Otherwise, it waits for the 8 FLAG which signifies that the first 8 bits of the data word are latched in the 8-bit latch and are ready to be transferred. The subcontroller advances to state "r" where the 8 FLAG is set and DIGITAL READY is sent to the GPIB handshake subcontroller. The subcontroller waits in state "r" for the 4 SEC flag, upon which states "z" and "p" are executed, or 16 FLAG, which signifies that the second 8 bits of the data word are latched on the 3 bit latch and are ready to be transferred. On this condition state "s" is entered which resets 16 FLAG and issues DIGITAL READY. The subcontroller then returns to state "q" to continue its operation.

Implementation

The MDS diagram, state assignment, and NEXT STATE maps are shown in Figures 32 and 33. As in previous controllers, the D-type flip-flop implementation is used for the present state holding register. Also, as in the other subcontrollers, the simplest implementation for the input decoding logic is the multiplexer implementation. Since branching is done off of more than one input that is asynchronous to the subcontroller, the necessary inputs are latched. The output decoder is a 4 line to 10 line decoder. These outputs must be latched to prevent flashing due to non-unit distance state assignments in some places. Schematics for this circuit are shown in Figure 34.

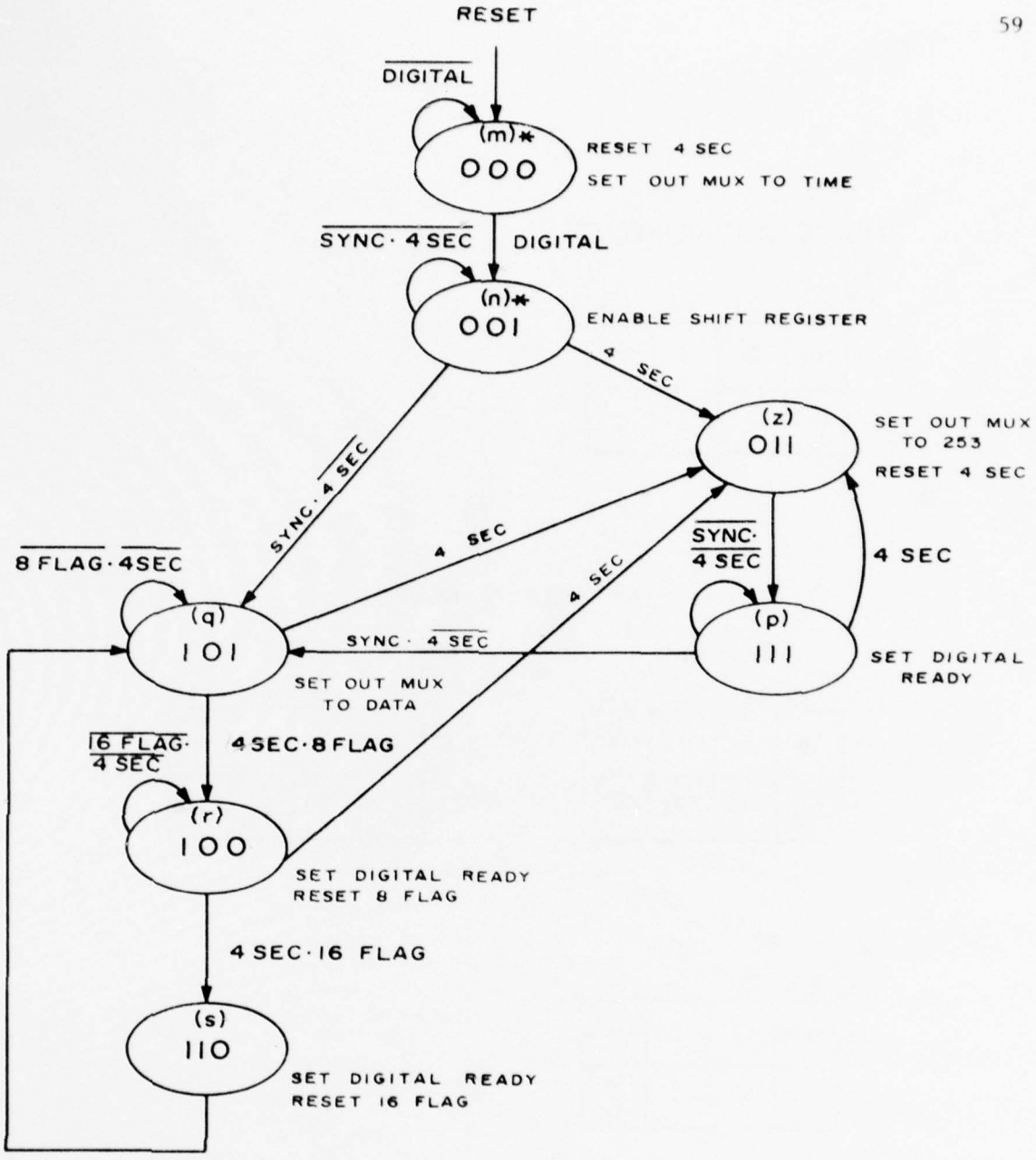


Figure 32. Main Digital Data Subcontroller: MDS Diagram

STATE ASSIGNMENT

A B / C	00	01	11	10
0	m	Ø	s	r
1	n	z	p	q

NEXT STATE MAPS

D_A (MSB)

A B / C	00	01	11	10
0	0	0	1	4 SEC
1	SYNC · $\overline{\text{4 SEC}}$	1	$\overline{\text{4 SEC}}$	$\overline{\text{4 SEC}}$

D_B

A B / C	00	01	11	10
0	0	0	0	4 SEC + 16 FLAG
1	4 SEC	1	4 SEC + $\overline{\text{SYNC}}$	4 SEC

D_C (LSB)

A B / C	00	01	11	10
0	DIGITAL	0	1	4 SEC
1	1	1	1	$\overline{\text{8 SEC}}$ + 4 SEC

Figure 33. Main Digital Data Subcontroller: State Assignment and NEXT STATE Maps

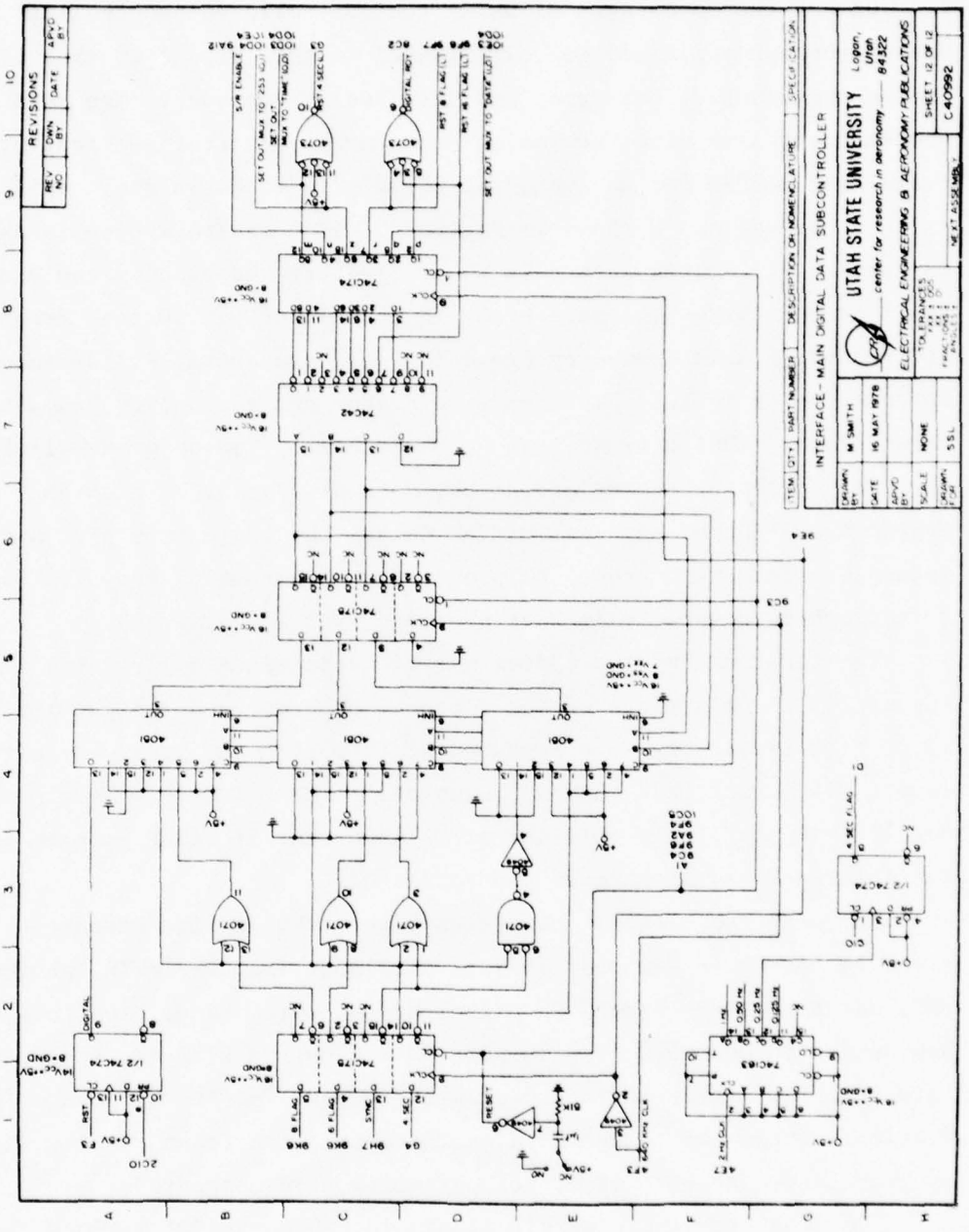


Figure 34. Main Digital Data Subcontroller: Schematics

RESULTS OF FIELD TESTING OF INTERFACE SYSTEM

One of the advantages of using the controller-subcontroller design concept explained and illustrated in this report is that a system can be constructed, debugged, and operated in sections. The main system controller with the analog section was constructed first since these were needed for an impending field trip to Kwajalein. This part of the system is shown in Figure 35. The entire system is shown in Figure 36. Programs to plot the trajectory and process and plot the data for the Capacitance Probe (C Probe), Direct Current Probe (DC Probe), Plasma Frequency Probe (PFP), Photometers, Field-Widened Interferometer (FWIR), Electron Accelerator and the Energy Deposition Scintillator (EDS) were written by David Burt. The programs allow the user to plot the complete flight data of a probe or plot an expanded section of any part of the data. The trajectory plot and data plots for the C probe, DC probe, and a photometer shown in Figures 37 through 39 respectively were produced by these programs.

The first use of the system was at Kwajalein Missile Range in August 1977. Data plots of the C probe, DC probe and two photometers along with trajectory were produced at this time and included in the report *Quick Look Field Report, Equatorial Irregularities-Wide Band Satellite Support*. In this operation a current limiting problem in the interface was discovered and corrected.

The next two uses of the system were at Poker Flat Research Range in Alaska in November 1977 to plot data from the FWIR, photometers, EDS, and the three-channel DC probe; and at White Sands Missile Range New Mexico in December 1977 to plot data from the Electron Accelerator. Data from the latter is included in the report *PRECEDE II: Summarized Results*. These two trips revealed the need for a front panel switch debounce and a reset switch; both of which were corrected.

The most recent use was in Alaska in February 1978. Plots of the trajectory, DC probe and PFP were included in *Quick Look Field Report, Coordinated Daytime Investigation of High Latitude Scintillations* on the Honest John-Hydac Wideband Rocket. Plots of the trajectory, Electric Field Probe, EDS, C Probe, and 2 photometers from the

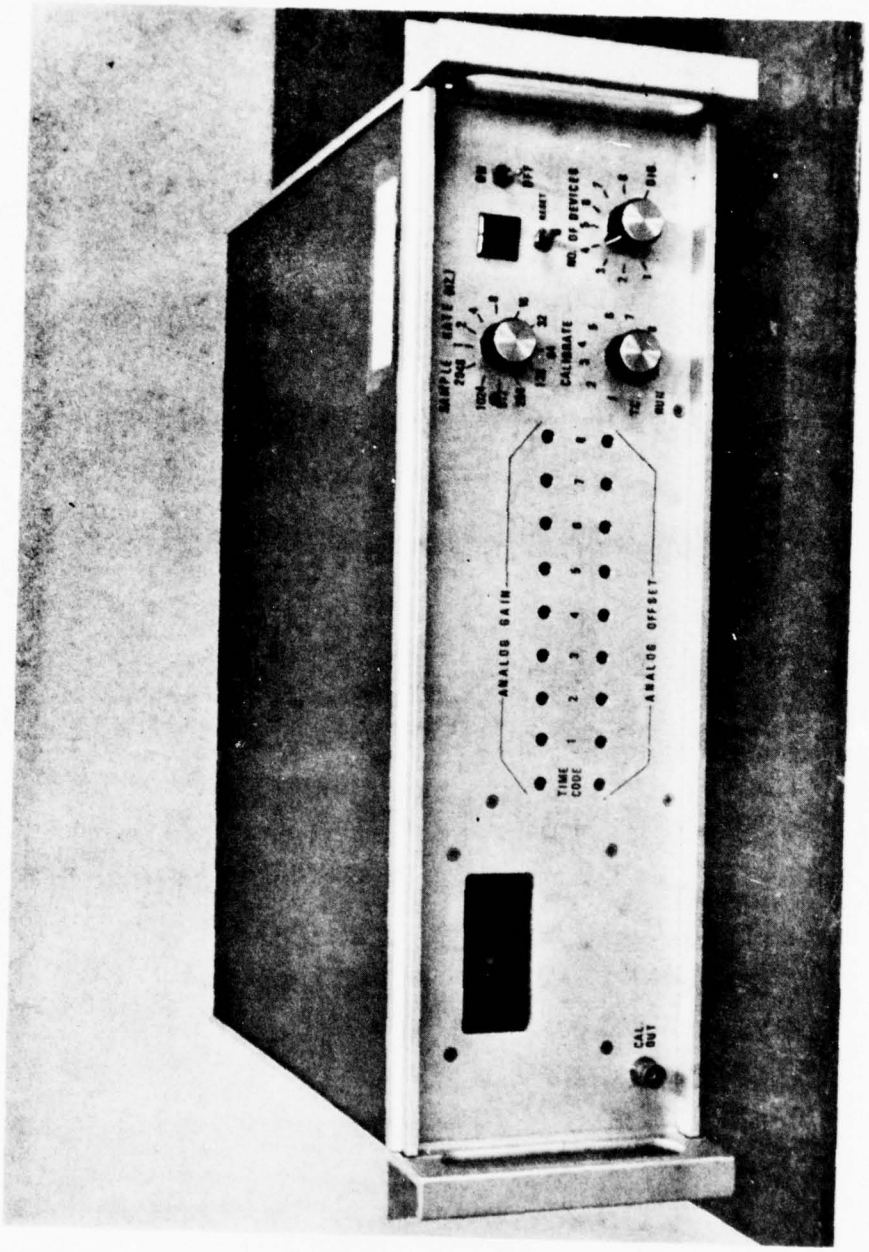


Figure 35. Picture of Interface

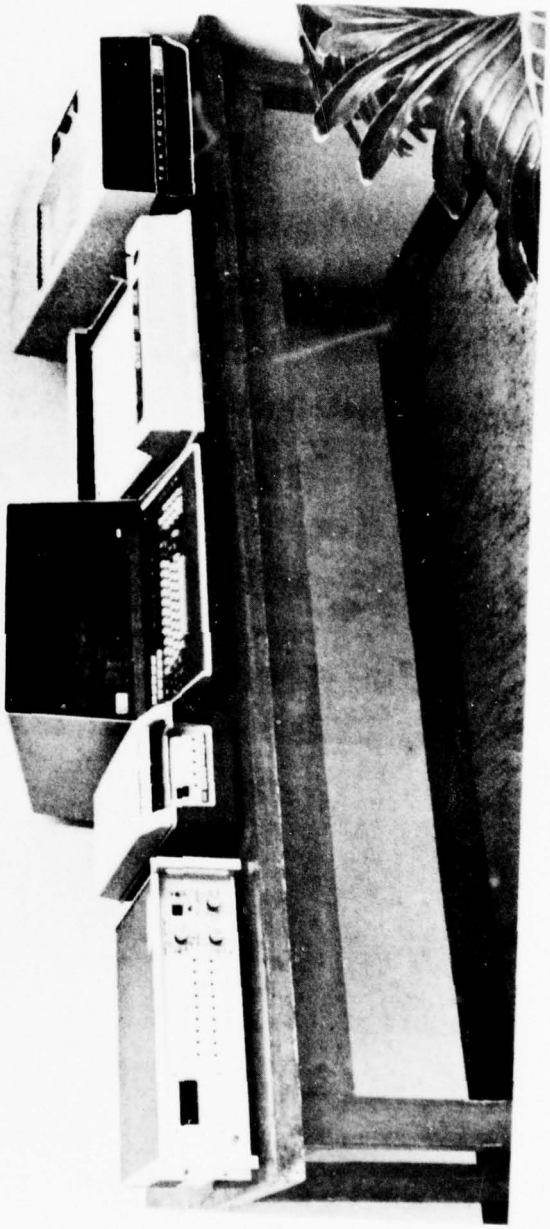


Figure 36. Picture of Complete System

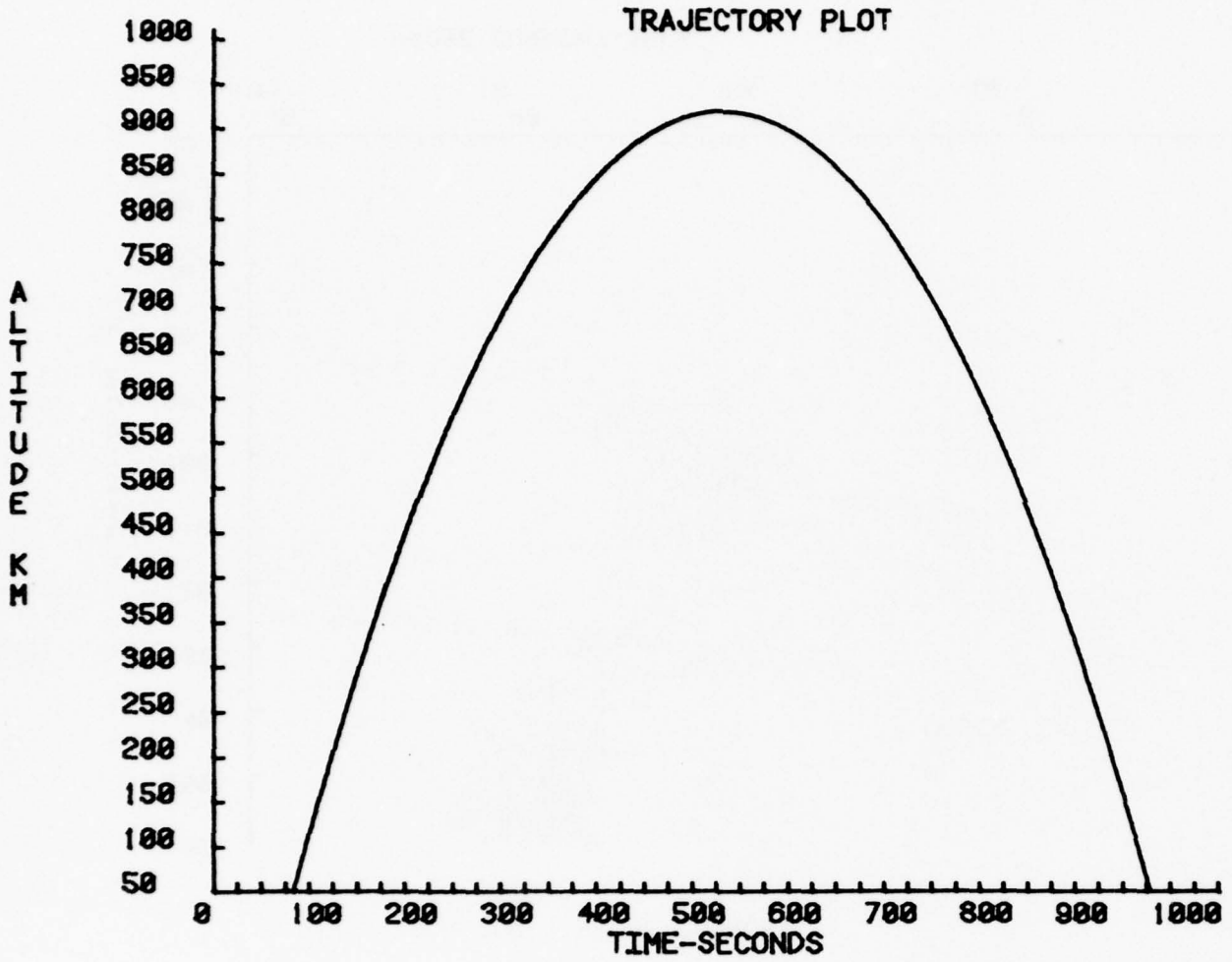


Figure 37. Trajectory Plot

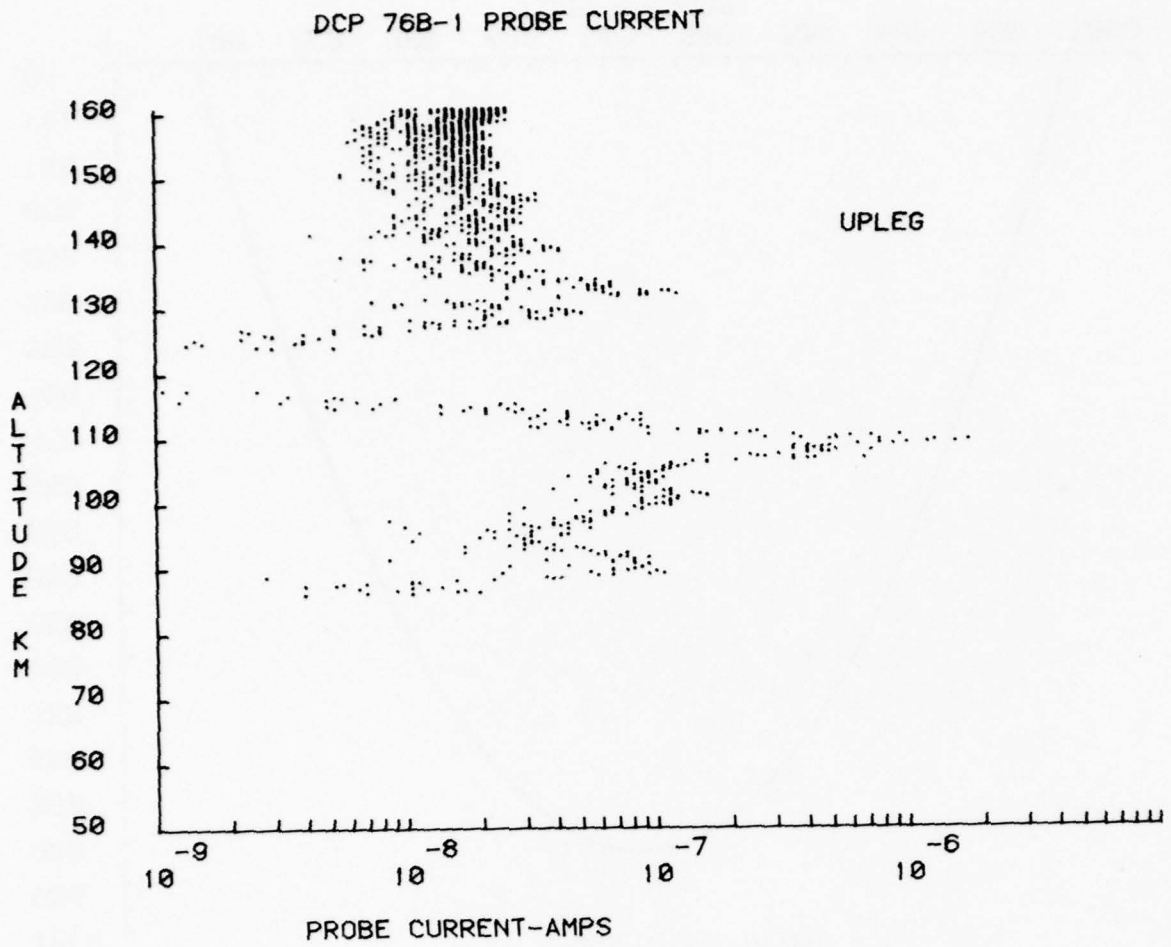


Figure 38. DC Probe Data Plot

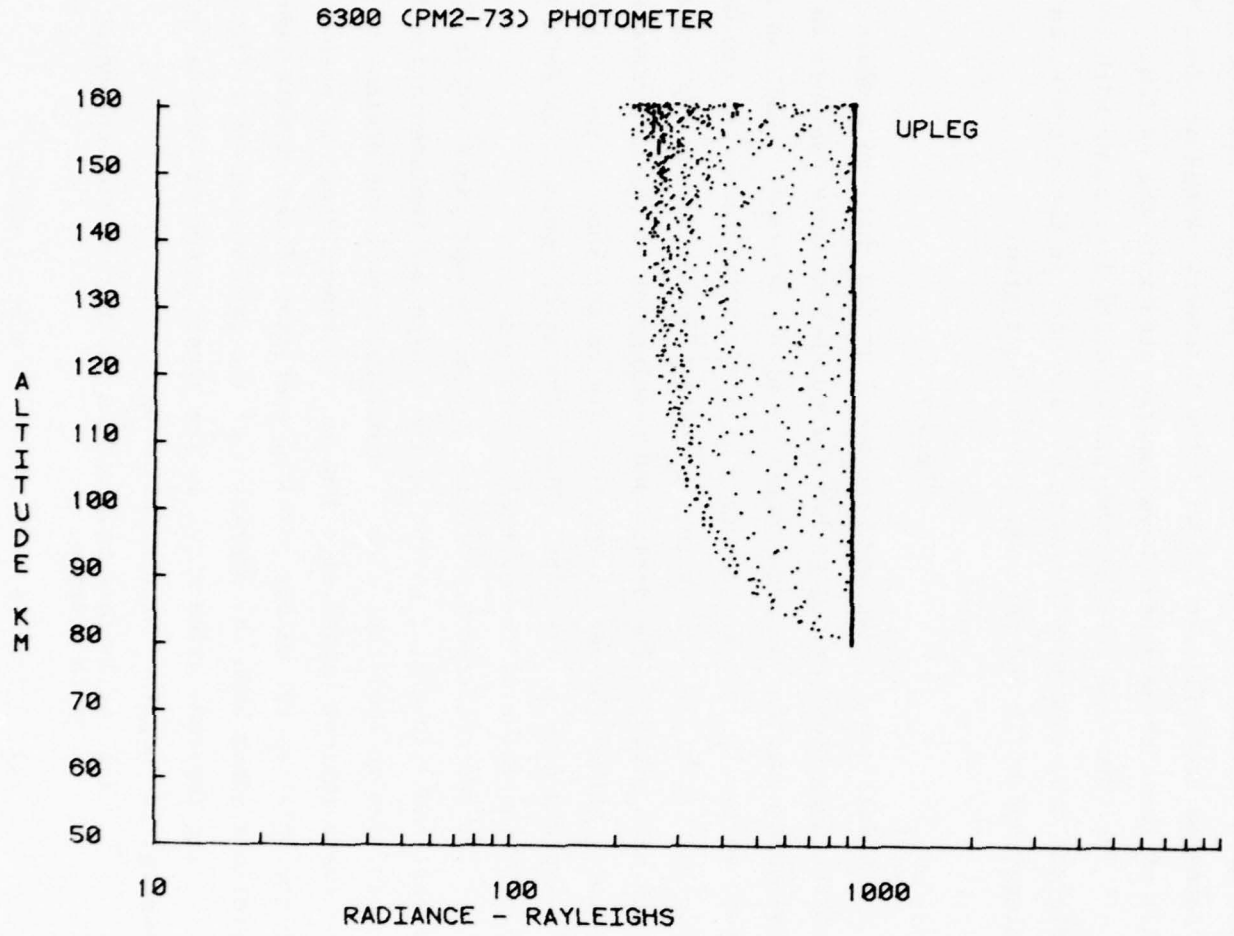


Figure 39. Photometer Data Plot

SGT-Hydac Multi-Rocket were included in *Quick Look Field Report, Coordinated Investigation at High Latitude Scintillations*. No problems were encountered in the operation of the interface itself, but more attenuation of the input signal and signal limiting were requested to facilitate use with the telemetry ground stations there. All of these changes have been incorporated into the system.

The IRIG time code decoder and subcontroller along with the digital data subcontroller were not included in these tests, but have since been built and integrated into the system.

Summary

A data acquisition and processing system that can produce plots of the data from various probes for quick-look data analysis is a valuable asset for persons concerned with the probes. With an interface system to transfer the data in a specified format to the 4924 Digital Cartridge Tape Drive, the 4051 Graphics System can produce such data plots. The design and development of the interface system meeting all of the design requirements established in the introduction is explained in this report. The plots in the quick-look data reports verify the value of the system's operation.

The controller-subcontroller design concept explained in this report and illustrated by the system design and implementation is a useful design tool that aids in simplifying both the design and hardware implementation of a system. Increased speed is also obtained since this concept allows parallel operation of one or more subcontrollers along with the operation of the main system controller.

The implementation shown in the thesis based on this design concept is comprised of the following:

(1) A 12-state main system controller with an analog data routine.

(2) A 4-state GPIB handshake subcontroller.

(3) A 5-state IRIG time code subcontroller and 7-state IRIG time code decoder.

(4) A 7-state main digital subcontroller and a 6-state synchronization detector.

A total of 41 states are used to implement this system. If the system was implemented with a single controller, an estimated 66 states would be required. This would complicate the design phase due to the many state variables involved, and increase the complexity of the input decoder, present state holding registers, and the output decoding logic. This shows that the design concept is very useful in applications where multiple control operations are required.

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Tektronix, Inc., *4662 Interactive Digital Plotter, Users' Manual*, 070-1932-01, p. Frontispiece, 1-1, 1-2, Tektronix, Inc., Beaverton, Oregon, June 1976.

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APPENDIX A

4051 Graphics System and Peripherals

4051 System Block Diagram Description

The 4051 Graphic System is a microcomputer system containing a Microprocessing Unit (MPU), a Random Access Memory (RAM), and a Read Only Memory (ROM). There are three built-in peripherals which attach directly to the MPU bus lines. These peripherals are the keyboard (the primary input device), the display (the primary output device), and the magnetic tape unit (a mass storage device). Two optional peripherals can also be attached via external plug connections: a Hard Copy Unit for making paper copies of displayed information, and a Joy Stick which allows the keyboard operator to manually control the position of the display cursor when entering graphic information.

There are two interfaces which provide a communication channel for external peripheral devices. The General Purpose Interface provides a bit-parallel, byte-serial data path for peripheral devices such as digital X-Y Plotters, Instrumentation Systems, and Disk File Devices. This interface conforms to IEEE Standard #488-1975. The Data Communications Interface provides a bit-serial link between the Graphic System and devices such as host computers, and modems. This interface conforms to the RS-232-C standard.

System Operation

The Graphic System receives, stores, solves, displays, and transmits logic problems that you create from a combination of symbols, letters, numbers, and graphics. The system accepts data from its keyboard, from magnetic tapes, and from other instruments. It displays data on its T.V.-like screen and it transmits the data to another instrument, to magnetic tape, or both simultaneously.

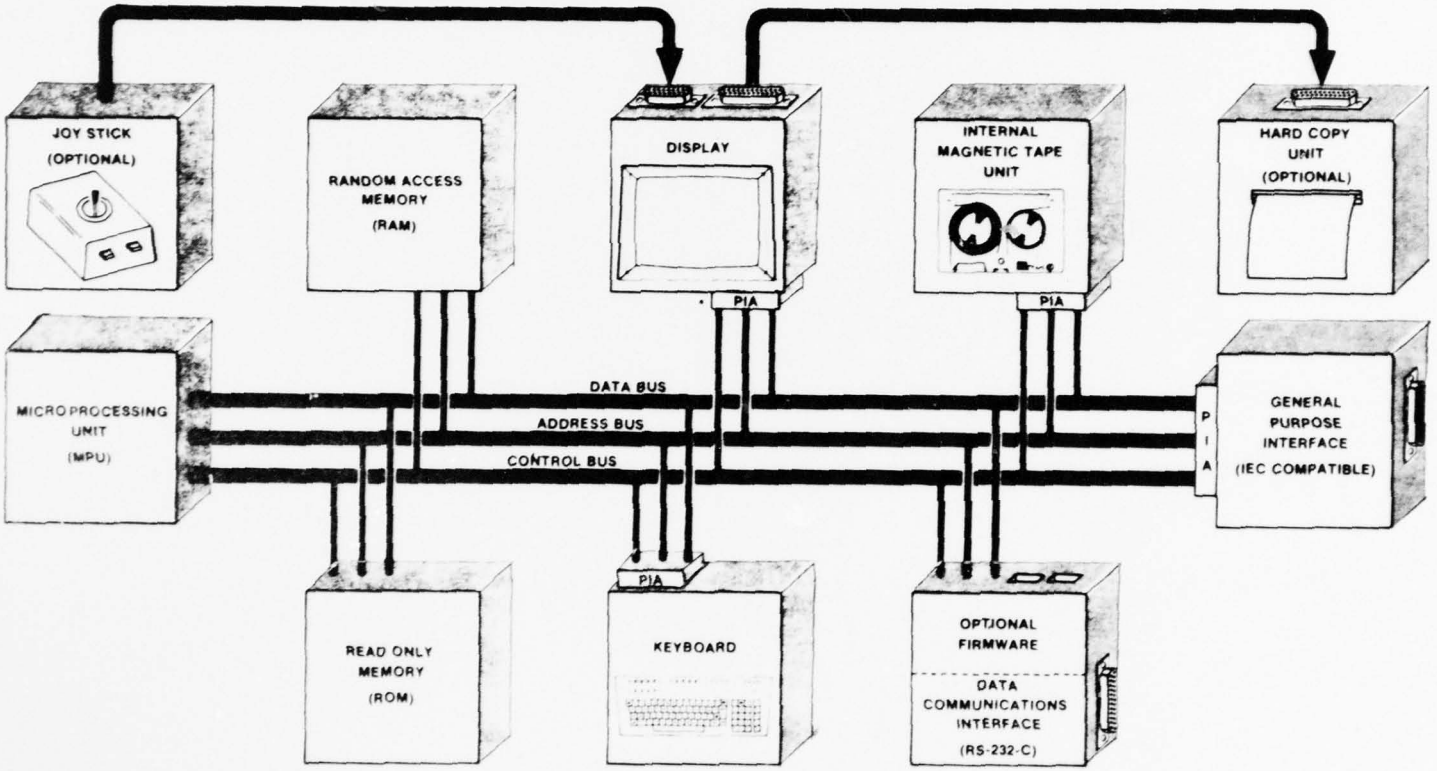
4662 General Description

The 4662 (Figure A3) is an Interactive Plotter that is digitally stepped and controlled. It provides permanent graphic recording capabilities for devices that have either the RS-232-C interface (such as Tektronix 4010-series Terminal based system) or the GPIB(IEC)[1]

[1]The GPIB interface is defined in IEEE Standard 488-1975; IEEE Standard Digital Interface for Programmable Instrumentation. A description of interface characteristics is found in Appendix B.

Figure A1. 4051 Graphics System

SYSTEM DESCRIPTION



4051 GRAPHIC SYSTEM

Figure A[illegible]. 40[illegible] System Description

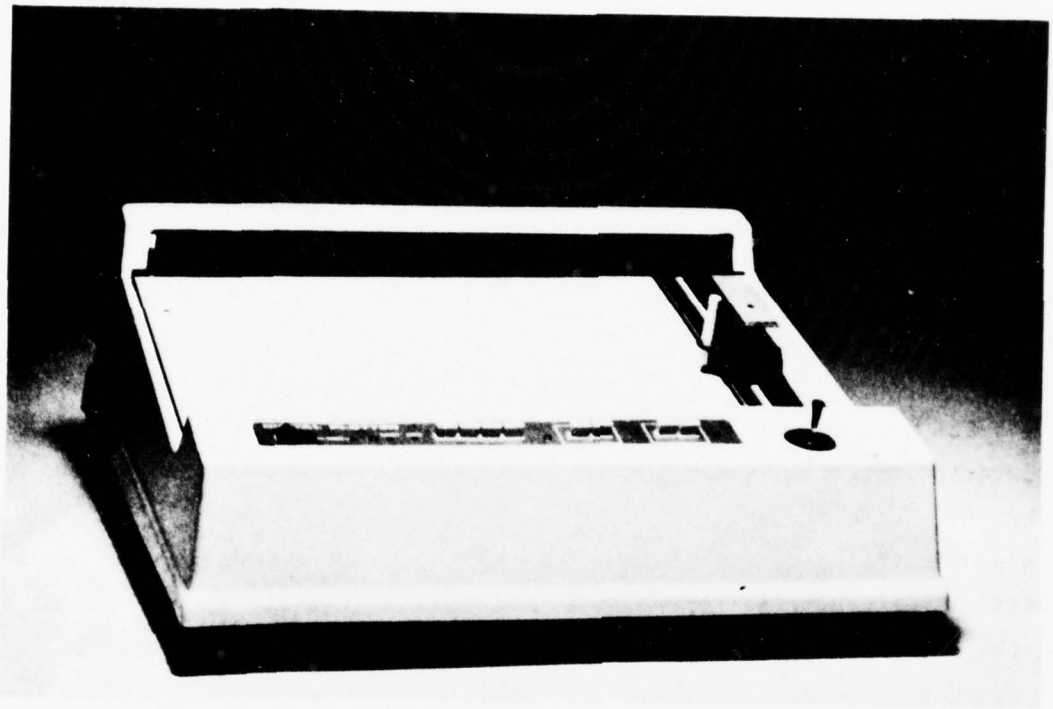


Figure A3. 4662 Interactive Digital Plotter

interface (such as the Tektronix 4051 Graphic System). This choice of interfaces allows the Plotter to be used with a wide variety of systems and equipment.

Each axis of the plotter is propelled by a four-phase stepping motor. Each motor pulley drives a plastic-covered cable that is attached to the pen carriage to move the carriage along the appropriate axis. Internal circuitry controls the number of steps in each axis to create the appropriate vector. Each motor step results in .005 inch of linear motion in that motor's axis.

The 4662 will accept paper sizes up to 11 inches (27.9 cm) in Y by 17 inches (43.2 cm) in X; maximum plotting size is 10 inches (25.4 cm) by 15 inches (38.1 cm). The Page Scaling feature of the 4662 allows the plot size to be easily adjusted from the front panel to fit the paper size being used. The paper is held in position by electrostatic attraction generated by the platen.

The 4662 performs three basic types of operations. It can print alphanumeric characters drawing the ASCII character received on the plotting surface. The Plotter can also produce graphics by moving the pen across the plotting surface, lifting and lowering the pen to produce written vectors only when desired. In addition, the (Graphic Input) GIN operation allows the Plotter to act as a digitizer, transmitting the coordinate position of the pen along with pen status (up or down) upon command. Actual implementation of these operations varies according to the interface being used.

Other features of the 4662 include the ability to scale the alphanumeric character sizes (independently from the plot size) and to rotate the alphanumeric characters. In addition, a number of plotters may be linked together with different device addresses assigned to each. In this way, data may be sent to only one of a group of plotters, selectively.

4924 General Description

The 4924 is a Digital Cartridge Tape Drive unit. By acting as a peripheral tape memory, it provides the capability for local storage of digitally-recorded data. The data is recorded on a 3M^{R} DC-300-A type of data cartridge.

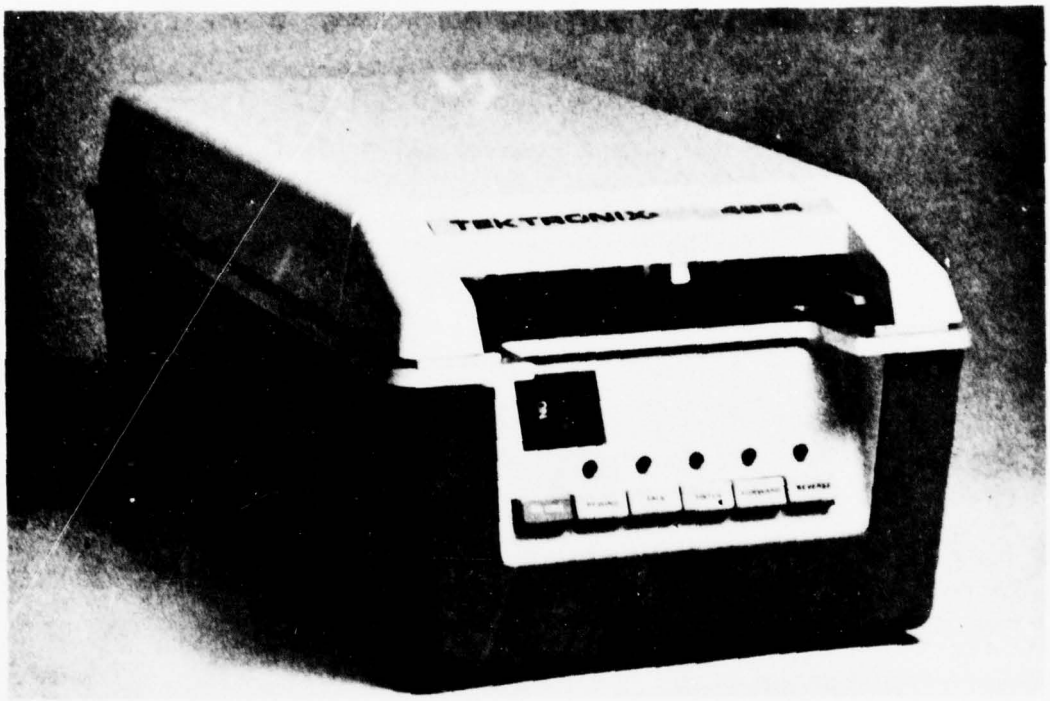


Figure A4. 4924 Digital Cartridge Tape Drive

The 4924 is equipped with a GPIB(IEC) interface for all input and output functions. This allows the 4924 to operate as an auxiliary storage device with systems that employ this type of interface. Such a system might include a system controller, such as a TEKTRONIX 4051 Graphic System, or might be a simpler instrumentation system containing only talkers and listeners.

There are two methods of controlling tape operations in the basic unit. One method employs commands issued over the GPIB. This method is typically used in GPIB systems that use a controller device, such as a TEKTRONIX 4051 Graphic System, to oversee system operation. The other control method employs front panel controls to perform basic tape operations. In addition, machines with Option 37 provide an alternate method of program-controlled operation. The operating method is selected by setting the front-panel ON LINE switch, and by the rear-panel switch on Option 37 units.

4631 General Description

The 4631 Hard Copy Unit (Figure A1) makes permanent high-contrast copies from Tektronix 4010-family Storage Display Terminals and Tektronix 613 and 613-1 Storage Display Units. A copy is produced when a remote copy command is applied, or when the COPY button on the front panel is pressed.

After the image is applied to the paper (as it passes in front of the CRT within the unit), the paper is cut and the image is heat-developed within the processor. The paper copy is then ejected into the paper tray in the top of the cover.

Figure A5. 4631 Hard Copy Unit

APPENDIX B

General Purpose Interface Bus (GPIB)

GPIB Connector

The GPIB connector is located on the rear panel of the Graphic System main chassis. This connector allows external peripheral devices to be connected to the system. The devices must conform to IEEE Standard #488-1975 which describes a byte-serial, bit-parallel interface system for programmable measuring apparatus. The GPIB connector is a standard 24-pin connector such as an Amphenal Micro-Ribbon^{R} connector, with sixteen active signal lines and eight interlaced grounds. The cable attached to the GPIB connector must be no longer than 20 meters maximum with no more than fifteen peripheral devices connected at one time. The connector pin arrangement and signal line nomenclature is shown in Figure B1.

The GPIB Interfacing Concept

The GPIB is functionally divided into three component busses; an eight-line Data Bus, a three-line Transfer Bus, and a five-line Management Bus for a total of sixteen active signal lines. This bus structure is shown in Figure B2.

The transfer rate over the Data Bus is a function of the slowest peripheral device taking part in a transfer at any one time. The bus operates asynchronously with a maximum transfer rate of 250K bytes/second (one megabyte/second with tristate drivers). Both peripheral addresses and data are sent sequentially over the Data Bus. Once peripheral addresses are established for a particular transfer, successive data bytes may be transmitted in a burst for higher effective data rates.

Peripheral devices on the GPIB are designated as talkers and listeners. The Graphic System acts as the controller to assign peripheral devices on the bus as listeners and talkers. The Graphic System further assumes that it is the only controller on the bus and it has complete control over the direction of all data transfers. There is no provision in the Graphic System for other devices on the GPIB to take turns as controller-in-charge.

A talker is a device capable of transmitting information on the Data Bus. There can be only one talker at a time. The Graphic

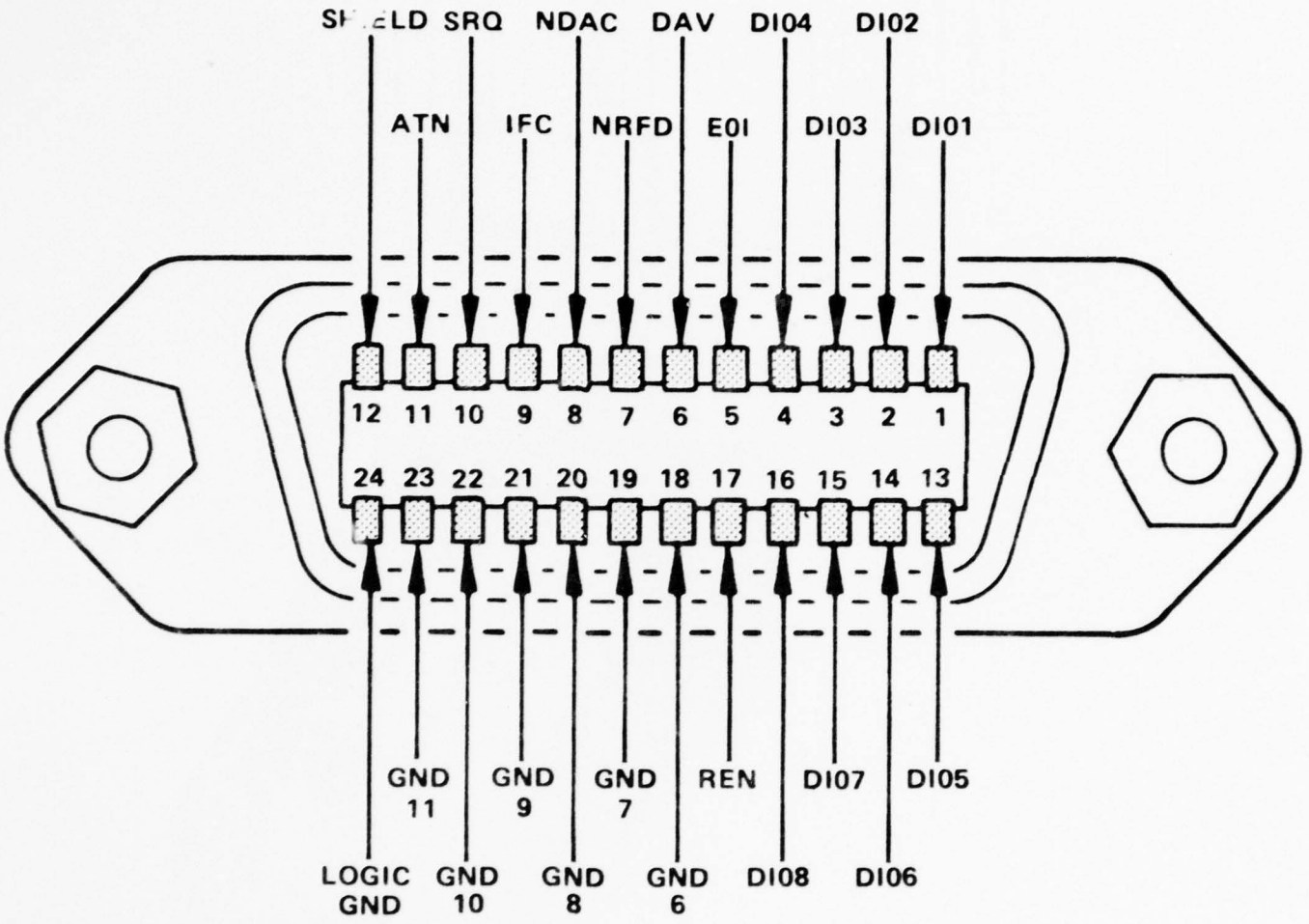


Figure B1. GPIB Connector

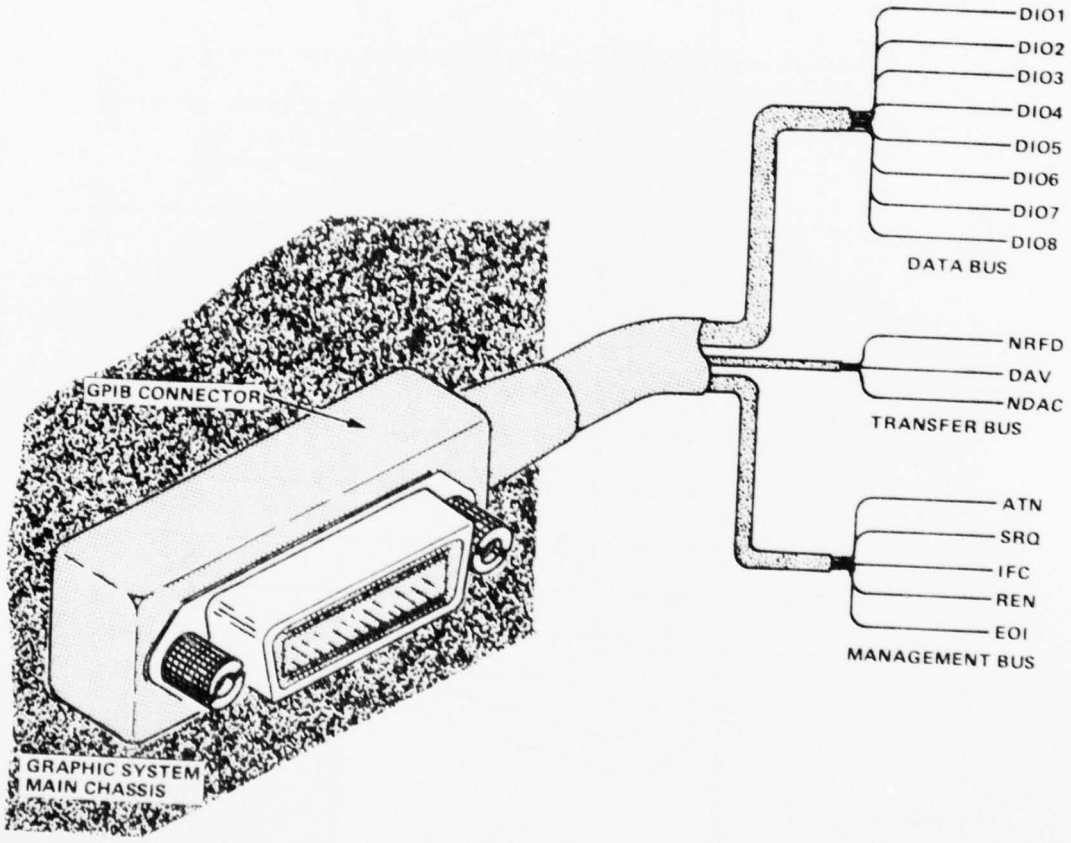


Figure B2. GPIB Bus Structure

System microprocessor has the ability to assume the role of the talker when it is programmed to do so.

A listener is a device capable of receiving information transmitted over the Data Bus. There may be up to fourteen listeners taking part in an I/O operation at any one time. The Graphic System microprocessor has the ability to assume the role of a listener any time it is programmed to do so.

GPIB Signal Definitions

Data Bus

The Data Bus contains eight bidirectional active-low signal lines, D101 through D108. One byte of information (eight bits) is transferred over the bus at a time. D101 represents the least significant bit in the byte; D108 represents the most significant bit in the byte. Each byte represents a peripheral address (either primary or secondary), a control word, or a data byte. Data bytes can be formatted in ASCII code, with or without parity (the Graphic System assumes no parity), or they can be formatted in machine-dependent binary code.

Management Bus

The Management Bus is a group of five signal lines which are used to control data transfers over the Data Bus. The signal definitions for the Management Bus are as follows:

SIGNAL	DEFINITION
Attention (ATN)	This signal line is activated by the controller when peripheral devices are being assigned as listeners and talkers. Only peripheral addresses and control messages can be transferred over the Data Bus when ATN is active low. After ATN goes high, only those peripheral devices which are assigned as listeners and talkers can take part in the data transfer. The Graphic System assumes it is the only source of this signal.

SIGNAL	DEFINITION
Service Request (SRQ)	Any peripheral device on the GPIB can request the attention of the controller by setting SRQ active low. The controller responds by setting ATN active low and executing a serial poll to see which device is requesting service. This response is generated b an ON SRQ THEN statement which is executed in the BASIC program. The serial poll is taken when a POLL statement is executed in the BASIC program. After the peripheral device requesting service is found, BASIC program control is transferred to a service routine for that device. When the service routine is finished executing, program control returns to the main program. The SRQ signal line is reset to an inactive state when the device requesting service is polled.
Interface Clear (IFC)	The IFC signal line is activated by the controller when it wants to place all interface circuitry in a predetermined quiescent state. The Graphic System assumes that it is the only source of this signal. IFC is activated each time the INIT statement is executed in a BASIC program.
Remote Enable (REN)	The REN signal line is activated whenever the system is operating under program control. REN causes all peripheral devices on GPIB to ignore their front panel controls and operate under remote control via signals and control messages received over the GPIB.
End or Identify (EOI)	The EOI signal can be used by the talker to indicate the end of a data transfer sequence. The talker activates EOI as the last byte of data is transmitted. When the controller is listening, it assumes that a data byte received is the last byte in the transmission if EOI is activated. When the controller is talking, it always activates EOI as the last byte is transferred.

The Transfer Bus

A handshake sequence is executed by the talker and the listeners over the Transfer Bus each time a data byte is transferred over the Data Bus. The Transfer Bus signal lines are defined as follows:

SIGNAL	DEFINITION
Not Ready for Data (NRFD)	An active low NRFD signal line indicates that one or more assigned listeners are not ready to receive the next data byte. When all of the assigned listeners for a particular data transfer have released NRFD, the NRFD line goes inactive high. This tells the talker to place the next data byte on the Data Bus.
Data Valid (DAV)	The DAV signal line is activated by the talker shortly after the talker places a valid data byte on the Data Bus. An active low DAV signal tells each listener to capture the data byte presently on the Data Bus. The talker is inhibited from activating DAV when NRFD is active low.
Data Not Accepted (NDAC)	The NDAC signal line is held active low by each listener until the listener captures the data byte currently being transmitted over the Data Bus. When all listeners have captured the data byte, NDAC goes inactive high. This tells the talker to take the byte off the Data Bus.

Handshake Parameter States

Once the CONTROLLER has assigned the TALKER and LISTENERS the data transfer may commence. The only activity on the bus should be the changing of DATA accompanied by the Data Valid variable (DAV) going from ϕ to 1 and the alternate switching of the NRFD (ϕ) and NDAC (ϕ) parameters from ϕ to 1 and back to ϕ again with the LISTENERS request for data (using NRFD) and, summarily, acceptance of data (using NDAC).

Two common errors may occur during the transfer. If a LISTENER requests data (NRFD = ϕ, NDAC = 1) and the TALKER never responds,

AD-A070 310 UTAH STATE UNIV LOGAN SPACE SCIENCE LAB F/G 9/6
DESIGN AND DEVELOPMENT OF A TELEMETRY LOGGING SYSTEM.(U)
JUN 78 M A SMITH F19628-76-C-0261
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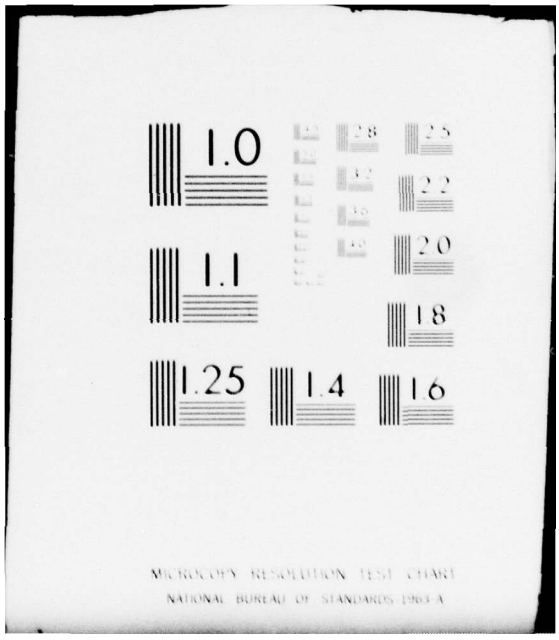
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MICROCOPY RESOLUTION TEST CHART
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which means not admitting that valid data is on the bus (DAV = ϕ), the bus will hang up. As there is no defined clocking rate for data, the LISTENERS think that they have a slow TALKER on the line and just sit there waiting for it. The difference between a slow talker and a dead one is a matter of degree. Thus, the controller cannot check for this error. This will occur during an incorrect INPUT, READ, OLD, or APPEND from an existing device or a request to TALK addressed to a LISTEN-only device.

The second error is more insidious. NRFD and NDAC are binary and the two can thus have a total of four different configurations (11, 10, 01, 00). Three are legal. The "0,0" state is a LISTENER error.

The "1,1" State

In the "1,1" state the LISTENER is Not Ready for Data (NRFD = 1) and has Not Accepted Data (NDAC = 1). This is a legal state for the LISTENER as it is indicating to the interface that it is not yet prepared internally to continue with the handshake cycle. If any LISTENER has the 1,1 configuration (NRFD (n) = 1, and NDAC (n) = 1) then communication on the bus is temporarily held up. All LISTENERS enter and leave communications modes in the 1,1 state.

The "ϕ,1" State

In the "ϕ,1" state the LISTENER is Ready for Data (NRFD = ϕ) and therefore Not Accepting Data (NDAC = 1). This is a legal state for any and all LISTENERS as it indicates to the interface and TALKER that the LISTENERS are prepared to receive messages.

The "1,ϕ" State

In the "1,ϕ" state the LISTENER is Not Ready for Data (NRFD =1) because it is in the process of Accepting Data (NDAC = ϕ). This is certainly a valid state as the LISTENER is indicating to the TALKER to maintain a valid byte of data. In the "1,0" state the LISTENER is indicating to the TALKER that it has received a data byte and is processing it.

The "ϕ,ϕ" State

The "ϕ,ϕ" state is always present in at least one device (the TALKER) but is not valid in an assigned LISTENER. In the "ϕ,ϕ" state the LISTENER is Ready for Data (NRFD = ϕ) and is in the process of Accepting Data (NDAC = ϕ). The first signifies to the TALKER to get rid of the present data and the second says to retain it as the data is still being read. The TALKER should recognize this as an error. Remember that the TALKER does not see the status of each LISTENER, but only the logical OR of all the NRFD (n) and all the NDAC (n) elements. If any LISTENER has its NRFD or NDAC parameter set to "1", the TALKER will not recognize the presence of a "ϕ,ϕ" state in another LISTENER. Sophisticated GPIB LISTENERS will generate an EOI or SRQ if both its NRFD and NDAC are "ϕ" and when the device is in the LISTENER mode. Many do not.

Handshake Sequence

Let us now consider the actual handshake sequence involving a TALKER (in control of parameter DAV) and some LISTENERS (controlling the communications rate with parameters NRFD and NDAC).

1. On initialization and just after assignment of TALKER and LISTENER status, the TALKER initializes DAV = ϕ(data not valid).

2. The LISTENERS initialize NRFD = 1 (none are ready for data) and set NDAC = 1 (none have accepted the data). The LISTENERS will hold up the system until they feel that they are able to handshake and respond to data if accepted.

3. The TALKER checks for the "ϕ,ϕ" status error condition (both NRFD and NDAC = ϕ) then places the DATA in the common area. In reality the data is placed on 8 parallel lines known as the DIO (Data Input/Output) lines.

4. The TALKER then delays to allow the data to "settle" on the DIO lines. Meanwhile the LISTENERS have initialized themselves and are capable of handshaking. They now wait until they are ready to accept data.

5. All LISTENERS have now indicated readiness to accept the first data byte (all NRFD (n) = ϕ), therefore, NRFD = ϕ.

6. The TALKER, upon sensing NRFD = ϕ, sets DAV = 1 to indicate that data is settled and valid.

7. The first LISTENER sets NRFD = 1 to indicate that it is no longer ready, then accepts the data. The other LISTENERS follow at their own rates.

8. The first LISTENER sets NDAC = ϕ to indicate that it has accepted the data. (NDAC remains = 1 because the other LISTENERS still have NDAC (n) = 1.)

9. The last LISTENER sets NDAC (n) = ϕ to indicate that it has accepted the data; all have now accepted and NDAC = ϕ.

10. The TALKER, having sensed that NDAC = ϕ, sets DAV = ϕ. This indicates to the LISTENERS that the data (on the DIO lines) must now be considered not valid.

11. TALKER changes data (on the DIO lines).

12. TALKER delays to allow data to settle (on the DIO lines).

13. LISTENERS, upon sensing DAV = ϕ (at 10) set NDAC = 1 in preparation for next cycle. NDAC = 1 as soon as the first LISTENER sets NDAC (n) = 1.

14. The first LISTENER indicates that it is ready for the next data byte (character) by setting NRFD (n) = ϕ. (NRFD remains = 1 due to other LISTENERS causing NRFD (ϕ) = 1.)

15. The last LISTENER indicates that it is ready for the next data byte by setting NRFD = ϕ. NRFD (ϕ) is now equal to ϕ.

16. The TALKER upon sensing NRFD = ϕ, sets DAV = 1 to indicate that data on the DIO lines is settled and valid.

17. The first LISTENER sets NRFD = 1 to indicate that it is no longer ready, then accepts the data.

18. The first LISTENER sets NDAC (n) = ϕ to indicate that it has accepted the data as in (8).

19. The last LISTENER sets NDAC = ϕ to indicate that it has accepted the data as in (9).

20. The TALKER, having sensed that NDAC (ϕ) = ϕ, sets DAV = ϕ as in (10).

21. The TALKER removes the data byte from the DIO signal lines after setting DAV = ϕ.

22. The LISTENERS, upon sensing DAV = ϕ, set NDAC = 1 in preparation for the next cycle.

23. Note that all three handshake signals, DAV, NRFD and NDAC are at their initialized states as in (1) and (2).

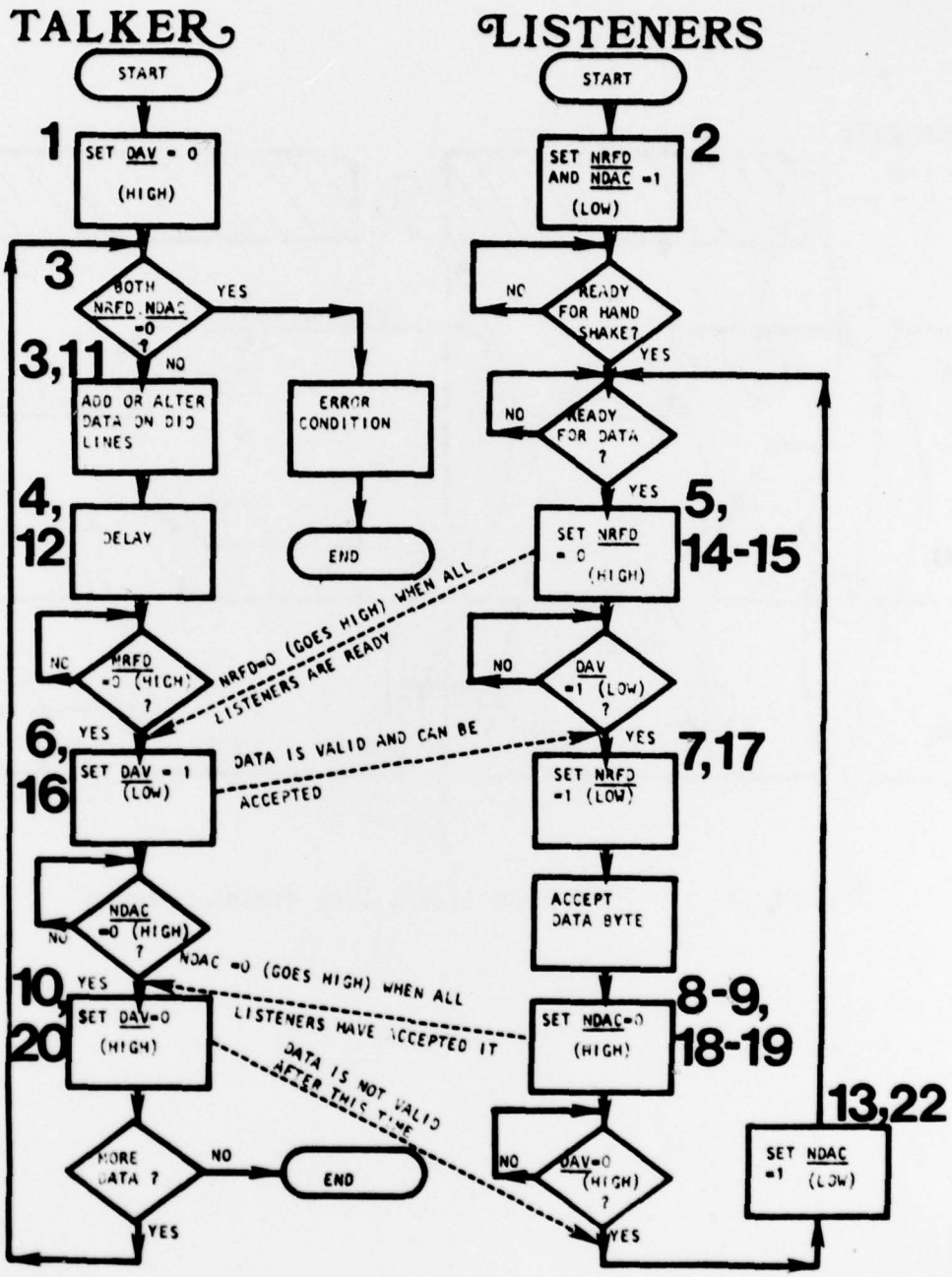

Figure B3. GPIB Handshake Sequence

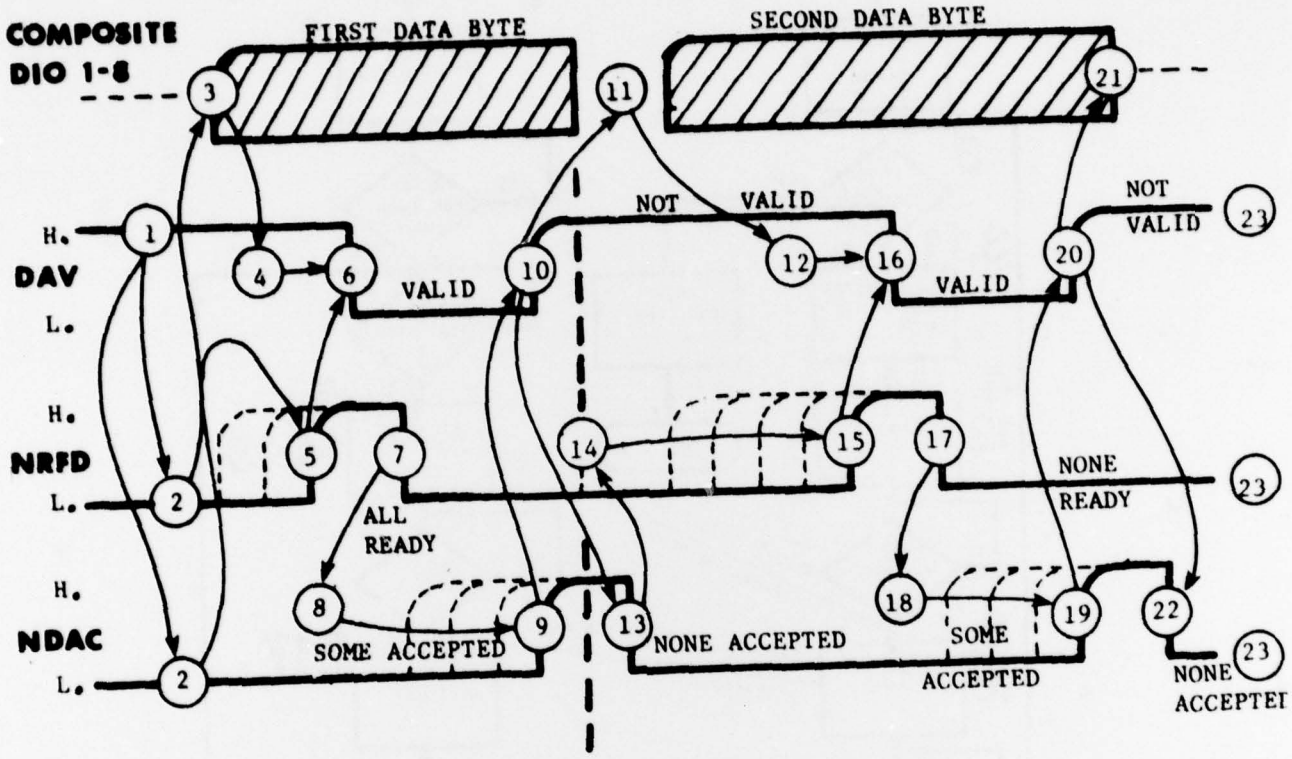

FIGURE B4. HANDSHAKE SIGNAL LINE TIMING SEQUENCE

APPENDIX C

IRIG Time Code, Format B

IRIG Format B

1. Time: Universal Time (UT-2).
2. Time Frame: 1.0 second.
3. Code Digit Weighing Options: BCD, SB or both.
   a. Binary Coded Decimal time-of-year Code Word--30 binary digits.
      1. Seconds, minutes, hours, and days.
      2. Recycles yearly.
   b. Straight Binary time-of-day Code Word--17 binary digits.
      1. Seconds only.
      2. Recycles each 24 hours.
4. Code Word Structure:
   a. BCD: Word begins at Index Count! Binary coded elements occur between Position Identifier Elements (7 for seconds, 7 for minutes, 6 for hours, 8 and 2 for days) until the Code Word is complete. An Index Marker occurs between decimal digits in each group to provide separation for visual resolution.
   b. SB: Word begins at Index Count 80. Five decimal digits (17 binary coded elements) occur with a Position Identifier between the 9th and 10th binary coded elements.
5. Least significant digit occurs first.
6. Element rates available:
   a. 100 per second (basic Element rate).
   b. 10 per second.
   c. 1 per second.
7. Element Identification:
   a. "On time" reference point for all Elements is the leading edge.
   b. Index Marker.....2 milliseconds. (Binary zero or uncoded Element)
   c. Code Digit.....5 milliseconds. (Binary End).

d. Position Identifier--10 per second.....10 milliseconds.
(Refers to the leading edge of the succeeding Element.)

e. Reference Marker--1 per second.....2 consecutive Position Identifiers.
(The "on time" print, to which the Code Word refers is the leading edge of the second Position Identifier.)

8. Resolution: 10 milliseconds (unmodulated).
1 millisecond (modulated).

9. Carrier Frequency: 1 kc. when modulated.

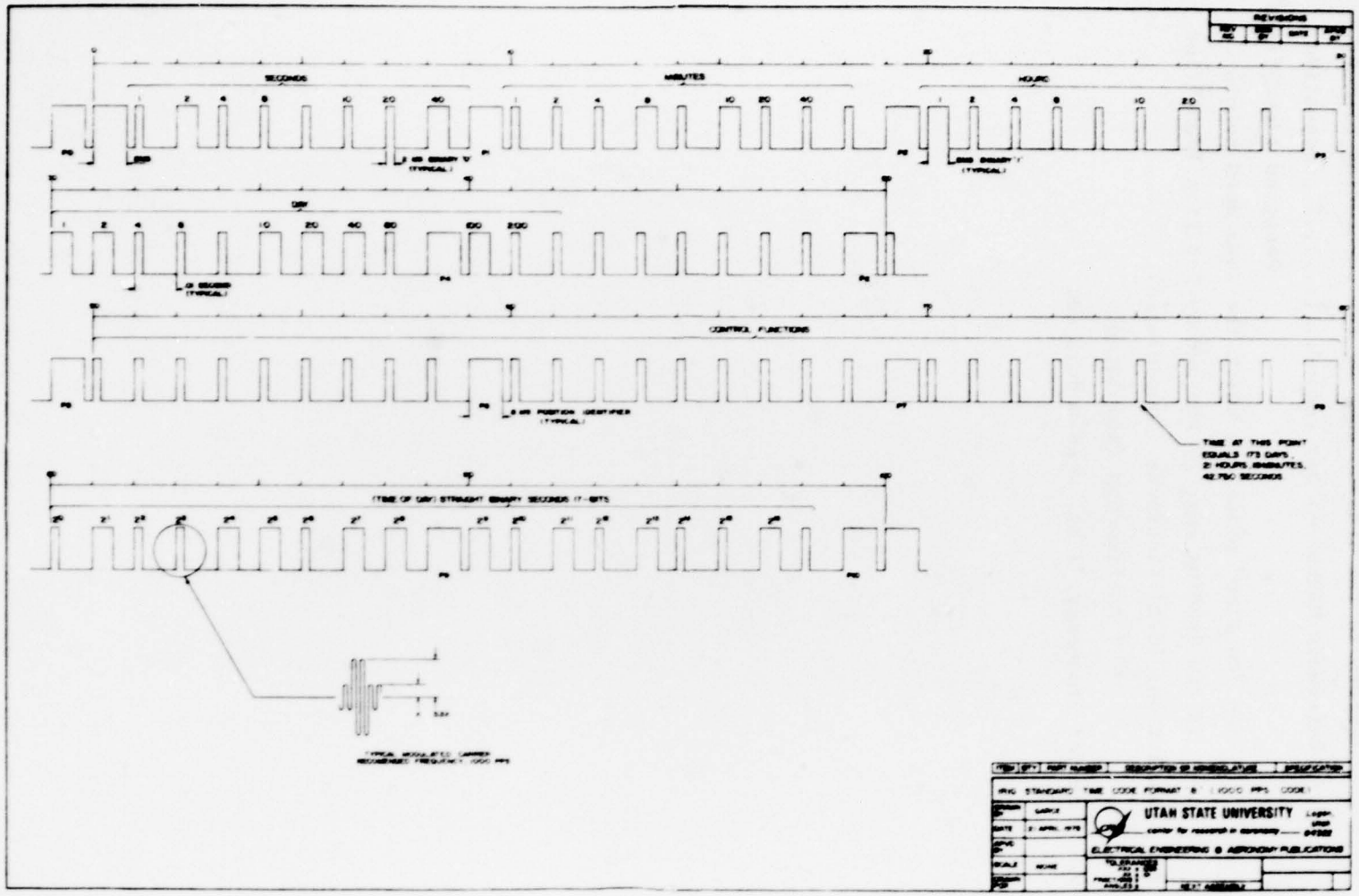

Figure C1. IRIG Standard Time Code Format "B"

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